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Reducing Beat Frequency Oscillation in a Two-phase Sliding Mode-controlled Voltage Regulator Module

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ABSTRACT

During static and dynamic loading conditions, voltage regulator modules (VRMs) are expected to provide regulated voltage with minimal ripple even at high current requirement. Compared to regular power supplies, VRMs repetitively experience high-frequency loading conditions that is greatly dependent on the software running in the processor utilizing them. In the scenario that when the transient load frequency is near the VRM's switching frequency, high-magnitude and low-frequency oscillations are observed at the phase currents. This phenomenon is called the beat frequency oscillation. In this study, the sliding mode control principle is employed to both the voltage and current share loops of the VRM to reduce the phase currents' beat frequency oscillations. A fixed frequency sliding mode controller is derived and extensively evaluated using the PSIM simulator. Our results show that while maintaining equal load sharing among VRMs at less than 5% sharing error and various types of loading conditions, the sliding mode controller can reduce the beat frequency oscillation phenomenon to 20 kHz at maximum with reduced peak current values. The output voltage is also regulated within the desired ±1.65% band.

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1. INTRODUCTION

The growing demands for high-speed and high-performance processors because of ubiquitous computing have dictated the digital market growth and provided various design challenges for the processors' voltage regulator modules (VRMs). Non-standard power supplies, i.e., supply voltage is less than 5 V, are providing the power requirement for these high-performance processors [1]. VRMs use the buck converter as they step down voltages from the main supply. Nowadays, VRMs have lower voltage outputs (0.6V to 1.5V) while providing higher output currents (130A to 150A) to satisfy the processor's speed and performance needs while operating at a switching frequency range of 0.2 – 1 MHz [2]. Another issue influenced by the processor speed and the various running softwares is the dynamic loading of the VRMs ranging from several kHz to several MHz while the load transient duration can be randomly fixed at one value for a certain period.

Another challenge is the high output current requirement of the VRM [3]. Most VRMs utilize a multiple-phase configuration to equally deliver the necessary high output current among its phases. A quasi-square wave VRM is a standard adopted by the industry for solving the fast transient and high output requirements [4]. A multi-phase buck converter implements parallel modules to achieve the high output current and transient demands, while not increasing the number of semiconductor devices. Having connected modules reduces the total equivalent inductance and output capacitance values. The ripple current is significantly smaller because the interleaved current phases cancel each other in magnitude.

VRMs must also maintain equal current sharing at any given repetitive load transient with frequencies equal to or higher the switching frequency. Load transients can reach up to 2 MHz and can even exceed the converter switching frequency. During a high repetitive high-frequency transient loading, a high-amplitude low-frequency oscillation, present at the phase currents of the inductors, can damage the VRM. This is known as the beat frequency oscillation (BFO) and occurs when the perturbation frequency is near the switching frequency [5]. The frequency of oscillation is determined as the difference between the switching frequency and the load transient frequency [6]. For video game software, BFO manifests in a low audible noise heard from the CPU. Another manifestation of BFO is the blue screening of the computer monitor. To eliminate BFO, [7] suggested to apply frequency modulation during transient conditions only. This is done to spread the beat frequency over the harmonics. In [8], the use of coupled inductors is recommended.

Various controllers have been employed to stabilize switched-mode power supplies. In [9], a comparison between the performance of a Proportional-Integral (PI) classical control method, fuzzy logic control and fixed frequency sliding mode control (SMC) is studied. SMC is a non-linear control approach that operates by choosing and directing the trajectory of state variables towards the desired equilibrium. The response of the system with the use of sliding mode control is guaranteed to be stable at all conditions and likewise independent of load and line changes [10]. On the other hand, the PI controller failed to deliver acceptable performance under load and line disturbances in contrast with the fuzzy and SMC controllers. By substituting linear controllers with SMCs, better performance against varying line and load disturbances, as well as better output voltage regulation can be achieved. However, despite the advantages of using SMC as a control method for DC-DC converters, it is rarely applied to DC-DC converters because of the infinite frequency requirement of SMC.

Many research studies have outlined and discussed how SMC is applied to the design of switching power supplies. M. Ahmed [11], developed a set of coarse guidelines for developing a buck converter employing SMC. In [12], a working prototype was developed, however, the power specifications are just 0.92 A at 12 V output, with a maximum overshoot of 700 mV. In [13], a constant ramp controller was introduced. Adaptive methods were developed in [14]. An adaptive feedforward control varied the hysteresis band for every change of line condition. On the other hand, load variation was improved by varying the sliding coefficients with every load change. In [15], design equations for hysteresis-modulation (HM) SMC were created but only applicable to voltage mode-controlled converters. Another set of research works have proposed of converting HM-based SMC to PWM-based SMC [16].

The application of SMC in mitigating the BFOs in VRMs is still an open research field [17]. An attempt to solve the start-up problem for VRMs and the output variation during high frequency transient were discussed in [18], but was still not able to address the BFO problem. Finally, the work in [19] also applied sliding mode to a VRM by having two loops of control depending on the trajectories of the error and its position in a defined boundary layer focusing only on the static and low frequency transient conditions.

In this research, we aim to reduce BFO by applying the SMC principles to both the voltage and current share loops. To the best of our knowledge, the study of eliminating beat frequency oscillation in multiphase voltage regulator modules is still very new. The work in [20] is the closest literature we can search but only deals with a single voltage regulator module and only use the voltage-mode control. The main contributions of this research work are discussed below.

1. Developed and implemented a fixed frequency sliding mode analog controller for a two-phase VRM. For a robust controller design, the fixed frequency sliding mode controller is applied to both the voltage and current-sharing control loops.
2. Reduced the beat frequency oscillations when implementing the SMC controller. The peak currents in each of the phases of the VRM did not reach twice its amplitude.
3. Extensive simulations evaluate the control performance and design robustness. Various loading conditions are used to test the designed controller, such as static and transient loading, and high-frequency transient loading.

The outline of the paper is as follows. Section 2 discusses how the converters of the VRM are designed and tested. Section 3 shows the derivation of the proposed SMC-based controllers. The simulation results are discussed in Section 4. Finally, the conclusion and future work are stated in Section 5.

2. CONVERTER DESIGN, TEST PROCEDURES AND SETUP

The design of the multi-phase VRM shown in Figure 1 with specifications given in Table 1 follows the continuous conduction mode equations. This ensures that the converter duty cycle is only affected by the input and output voltages and is independent with the load current. The reader is referred to [21] for the complete derivation of the inductor and capacitor values. We have assumed ideal inductor and capacitor values in our simulations of the multiphase voltage regulator module.

Table 1. Two-Phase VRM Specifications [2]

Specifications	Value	Specifications	Value
Input Voltage (V_{in})	12 V	Switching frequency (f_{SW})	300 kHz
Output Voltage (V_{out})	1.5 V	Current Sharing Accuracy	±5%
Output Regulation Band	±1.65%	Steady State Ripple Voltage	15 mVpk-pk
Voltage Ripple (V_{ripple})	15 mV	Transient Ripple Voltage	300 mVpk-pk
Maximum Load Current (I_{out})	80 A	Current Step	40 A
Minimum Load Current	1 A	Slew Rate	100 A/us

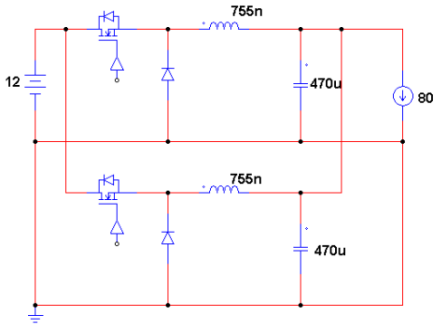


Figure 1. Two-phase Voltage Regulator Module

2.1. Test Procedure

The simulation tool used is PSIM® Software by Powersim because it is specifically designed for power electronics, analog and digital control, magnetic and motor drives. From the developed circuit, the following tests are done.

1) Voltage Regulation – the VRM is subjected to different load conditions to observe the output voltage. Load settings are 10% load (8A), half load (40A) and full load (80A), a shown in Figure 2 (a). Voltage regulation is set to 1.5 V ± 1.65%.
2) Transient Testing – the VRM step load response is tested at the maximum load step and under different slew-rate conditions. During this test, the overshoot and the undershoot are recorded. Figure 2 shows the load profile for such test.
3) High Frequency Loading Condition Testing – Beat frequency oscillation occurs when the load transient frequency is near the switching frequency of the power converter. The model will be subjected to load transients with frequencies of 290 kHz, 300 kHz, and 310 kHz. The high frequency load is characterized by a constant current slew rate of 100A/us with the load traversing from half load to full load with equal duty cycle for each current excursion. Figure 2 (b) shows the load profile for the high frequency loading condition test. Determining the presence of beat frequency is done by observing the inductor phase currents and looking for a low frequency oscillation at these phase currents.

For all simulation runs, the output voltage and phase currents are observed for stability and current sharing capabilities. The presence of beat frequency oscillation is observed at the phase currents of the two-phase VRM. Current sharing accuracy of ±5% is desired [22].

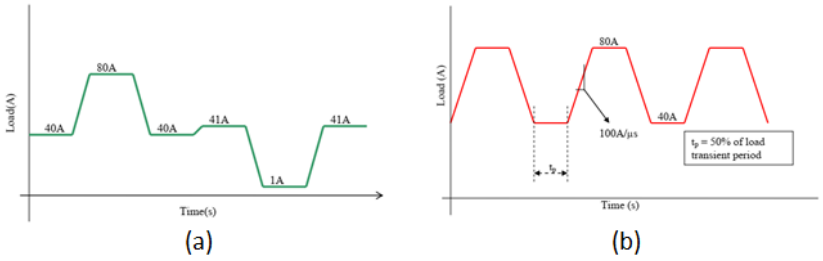


Figure 2. Load Profile for (a) Transient Testing and (b) High Frequency Load Condition

2.2. Test Setup

The designed VRM will be tested in accordance with Intel Voltage Regulator Down (VRD) 11.1 Processor Power Delivery Design Guidelines, where the LGA 775 Specifications will be used. Our rigid simulations have considered the bulk capacitors and high frequency filtering capacitance as well as the parasitic elements coming from the motherboard and socket interconnects.

3. SLIDING MODE CONTROL DERIVATION

Since this work focuses with the converter's voltage regulation and equal load sharing, the voltage and the current share loops must be controlled and stabilized. The voltage loop regulates the desired output voltage, while the current share loop handles the load sharing of the converters. In this study, the voltage-mode control and the average-current sharing method will be used to compensate the voltage and current loops, respectively.

3.1. Sliding Surface and State Variables

The state variables chosen to be controlled are the inductor current error (x_1) and voltage error (x_2). These two physical states are easily sensed in power supplies. The current error, x_1, determines if there is equal load current sharing between the modules. On the other hand, the voltage error, x_2, confirms that there is a regulated output voltage against any load variations. We define the current reference taken as the cumulative sum of all the inductor currents divided by the number of modules.

Ideally, if the SMC operates on an infinite frequency, both these errors tend to approach zero, therefore, achieving complete output voltage regulation and equal current sharing between the modules. However, since the frequency is set to a fixed value, these errors do not equate to zero, thus, we introduce a third state variable, i.e., the integral of the voltage error and the inductor current error, x_3, such that the steady-state errors are minimized. These three state variables are given in (1).

$$\begin{aligned} x_1 &= i_{ref} - \delta i_L \\ x_2 &= V_{ref} - \beta V_{out} \\ x_3 &= \int \left(i_{ref} - \delta i_L \right) dt + \int \left(V_{ref} - \beta V_{out} \right) dt \end{aligned} \tag{1}$$

where i_L, δ, i_{ref}, V_{ref}, V_{out}, and β are the load current, inductor current scaling factor, reference load current, output voltage reference, output voltage and voltage divider gain, respectively.

From these state variables, we define a linear combination that will determine our sliding surface, S, in (2), where the α_i's are the sliding coefficients to be determined for a stable operation of the VRM.

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 \tag{2}$$

3.2. VRM Dynamic Model and Equivalent Analog Control

The dynamic model of the VRM converter, employing the parallel buck converter configuration, is next determined. Since the logic of the switch dictates the state of the plant, the switching function, u (either 0 (switch is OFF) or 1 (switch is ON)), representing the switch must be taken into consideration. We define u by (3), where "sign" is the signum function.

$$u = \frac{1}{2}\left(1 + \text{sign}\left(S\right)\right) \tag{3}$$

From (1), the dynamic model of a buck converter is given by (4), where L and C are the inductance and capacitance values, respectively.

$$\dot{x}_1 = -\frac{uV_{in} - V_{out}}{L} \qquad \dot{x}_2 = -\beta \frac{i_C}{C} \qquad \dot{x}_3 = \left(i_{ref} - \delta i_L \right) + \left(V_{ref} - \beta V_{out} \right) \tag{4}$$

Differentiate (2), then substitute (4) to it and equate to zero to determine the equivalent sliding mode control, i.e., the switching function u as a function of the circuit parameters, given below in (5).

$$\begin{aligned} u_{eq} &= \frac{\delta V_{out}}{\delta V_{in}} - \frac{K_1 i_c}{\delta V_{in}} + \frac{K_2}{\delta V_{in}} \left[\left(i_{ref} - \delta i_L \right) + \left(V_{ref} - \beta V_{out} \right) \right] \\ K_1 &= \frac{\alpha_1}{\alpha_2} \frac{\beta L}{C} \quad \text{and} \quad K_2 = \frac{\alpha_3}{\alpha_1} L \end{aligned} \tag{5}$$

At steady state, i.e., $i_{ref} = i_L$ and $V_{ref} = V_{out}$ and $i_C = 0$, the control function u_{eq} reduces to the buck converter duty cycle, i.e., $u_{eq} = V_{out}/V_{in}$, when using the conventional linear controller. It is also noticeable that instead of having three sliding coefficients, we now only have two, i.e., K_1 and K_2, thus allowing us to design the control easier. K_1 is associated with the capacitor current, while K_2 ensures the voltage output regulation and the equal current sharing among the modules of the VRM. The PSIM block representation of VRM and sliding mode control is shown in Figure 3.

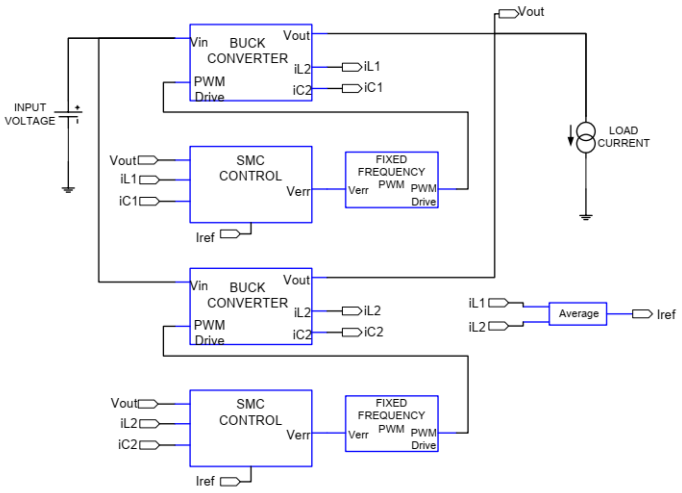


Figure 3. Block Diagram of the Sliding Mode Controller for a Two-Phase Voltage Regulator Module

To ensure that the state variables satisfy the hitting condition, it is necessary that the state variables' trajectory always stays inside the vicinity of the sliding manifold and that it is always directed towards the sliding manifold. By applying Lyapunov's direct method, we arrive at the existence condition for the VRM given by (6).

$$0 < \delta V_{out} - K_1 i_C + K_2 \left[\left(i_{ref} - \delta i_L \right) + \left(V_{ref} - \beta V_{out} \right) \right] < \delta V_{in} \qquad (6)$$

During steady state condition, the reference for both the output voltage and the inductor current as well as the capacitor current are equal to zero since it becomes an open circuit, effectively reducing to $0 < V_{out} < V_{in}$, which is an inherent characteristic of the buck converter. To determine the values of K_1 and K_2 that will ensure stability, (5) is substituted to the buck converter dynamic equations [23] to obtain the system's characteristic equation. Finally, after the application of the Routh-Hurwitz criterion, the values of K_1 and K_2 that will stabilize the system are given in (7).

$$K_2 \frac{\delta + \beta r_L}{CL\delta r_L} > 0; \quad \delta > -\beta r_L; \quad K_1 > -\frac{\delta L}{r_L} - \delta K_2 \qquad (7)$$

4. SIMULATION RESULTS AND DISCUSSION

The performance and the effectiveness of the derived SMC controller are evaluated through extensive simulations. We have chosen the control parameters K_1 and K_2 in (7) based on the minimum load condition values to ensure all loading conditions are covered. However, the actual control gains must be known iteratively, since the values are only given as a range.

4.1. Static Loading Condition Results

To determine the design and control robustness, the two-phase VRM is subjected to static loading where the output voltage, steady state ripple and current sharing are the parameters to be observed.

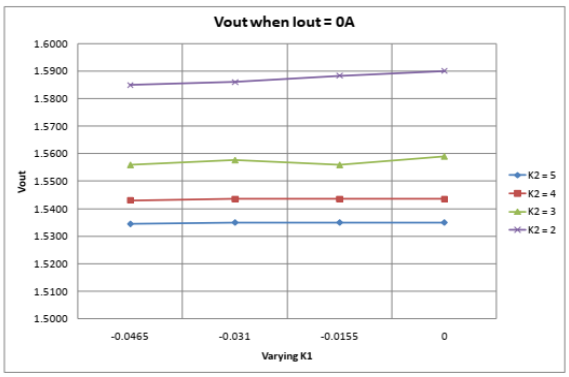


Figure 4. Output Regulation Behavior for Different Control Gains at No-load condition

4.1.1. Output Voltage Regulation

The loading points are taken at no load, 10%, 50% and 100% loading conditions. To determine if the results passed the test, the output voltage should be within V_{out} ± 1.65%. Figure 4 shows the regulation at no load condition. For values of K_1, the output voltage regulation is constant for any values of K_2. Increasing K_2 deteriorates the voltage regulation, but still regulates the converter's output voltage, implying that stability is achieved at no load condition.

Once the VRM draws load current, the behavior of the output voltage with respect to the control gains becomes slightly different, as manifested in

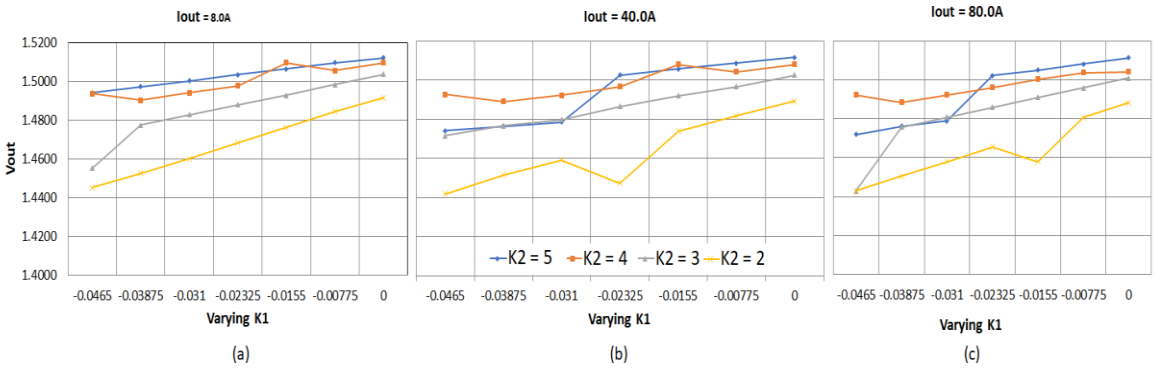


Figure 5. For a value of K_2, as K_1 approaches zero, the regulation improves compared to the condition when K_1 is negative. In

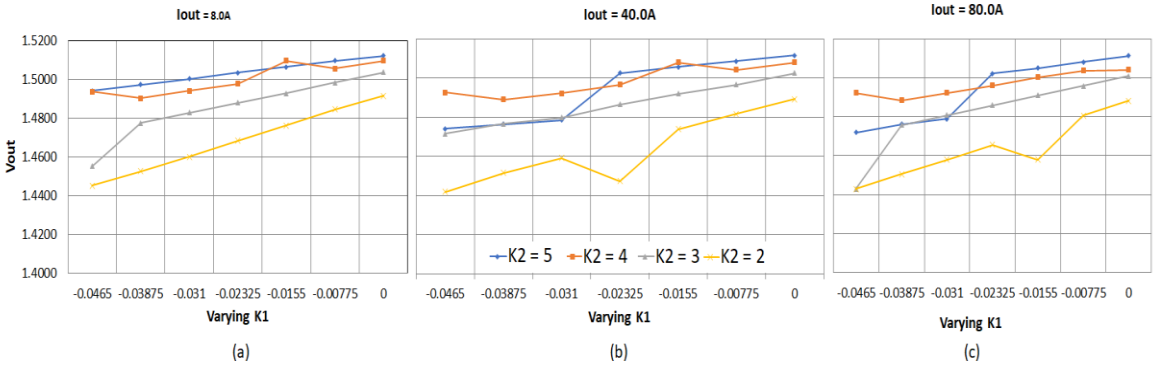


Figure 5(c), if K_2 = 2 and K_1 = -0.0465, the regulation is only 1.4420V against the 1.489 V regulation when K_1 = 0. Also, for a fixed K_1, the regulation is improved when K_2 is increased. In summary, K_1 monitors the current by capacitor sensing, while K_2 is directly responsible for the output voltage regulation of the VRM. The voltage error is reduced when there is a higher value of K_2.

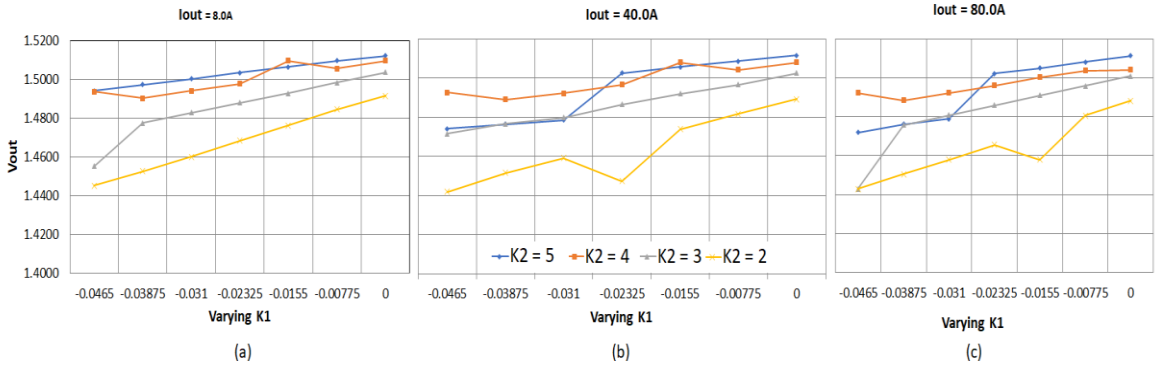


Figure 5. Output Regulation Behavior for Different Control Gains at (a) 10%, (b) 50% and (c) 100% loading conditions.

Figure 6 shows the waveforms of the output voltage and phase currents of the VRM for $K_2 = 4$, and $K_1 = -0.031$ depicting the stable operation of the SMC-controlled converters.

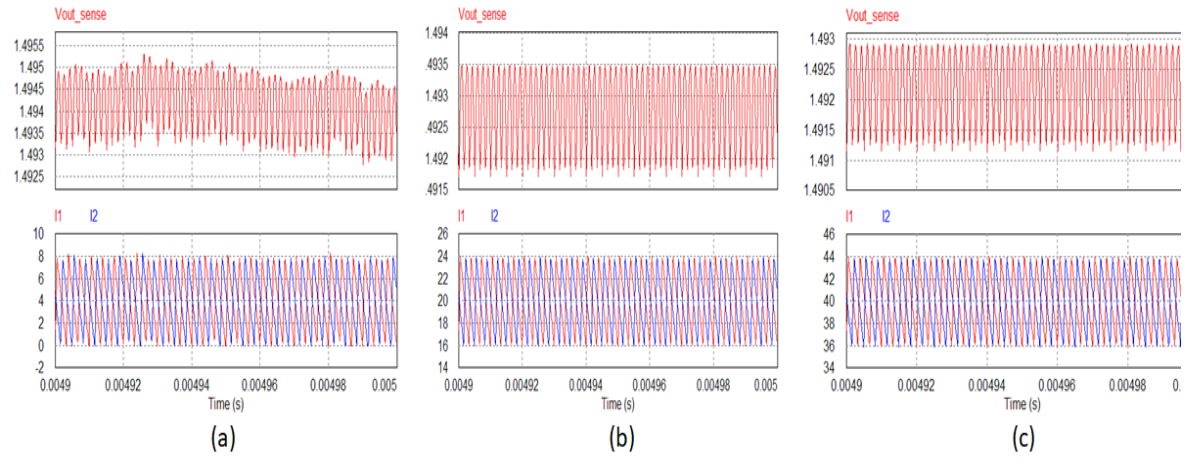


Figure 6. Operation of the VRM with *K2* = 4 and *K1* = -0.031 at (a) 8A, (b) 40A, and (c) at 80A load.

4.1.2. Output Ripple

The maximum allowed output ripple is set at 15 mV pk-pk [2]. Figure 7(a) shows the response of the VRM at 10% load. At all control gains, the output ripple is within the specifications, with the highest output ripple at 13.9 mV when the values of the control gains are $K_1 = -0.0465$ and $K_2 = 5$. At half load condition (Figure 7(b)), the behavior of the output ripple is constant except for $K_2 = 3$ and $K_2 = 5$. Ripple is generally independent of K_1. As seen from the plot, the ripple increase occurs with high K_2 value and with more negative K_1 value. During this portion the pulses of the converters are already "doubling", thus increasing the output voltage ripple. However, in other situations, the ripple remains constant even with varying K_1.

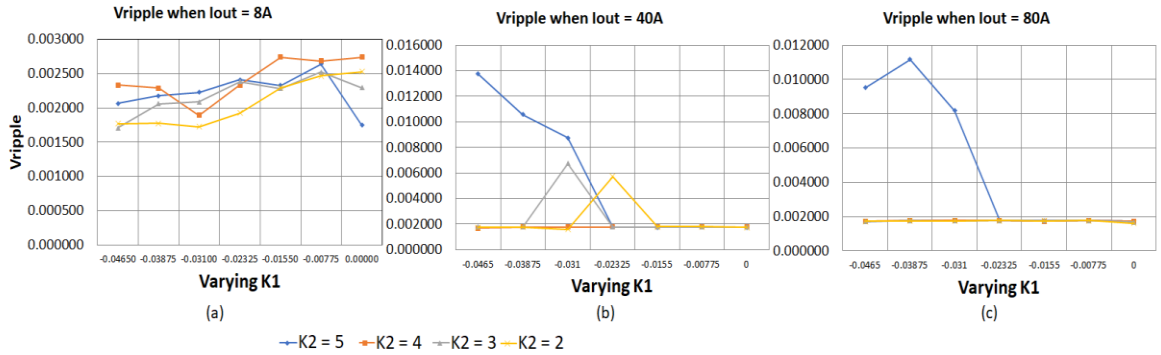


Figure 7. Output Voltage Ripple Behavior for Different Control Gains at (a) 10%, (b) 50% and (c) 100% loading conditions.

At full load condition, (Figure 7(c)), the response of the output voltage ripple is like the half load condition response. Ignoring the outlier from $K_2 = 5$, the output ripple voltage is constant for all control gains. The ripple voltage at both half load and full load conditions passes the 15mV pk-pk requirement of the VRM with a ~12mV margin. The outliers seen for the case of $K_2 = 5$, resulting in a high ripple voltage measurement, is due to issues observed in the control behavior of the converters. Upon inspection of the gate drive PWM, the pulses are no longer uniformly occurring. There are periodic sub-pulses occurring between the main pulses. Upon the occurrence of these pulses, the inductor current becomes distorted causing the high output ripple issues.

4.1.3. VRM Current Sharing

During static loading conditions, the current sharing between the phases of the VRM is recorded. The current sharing accuracy error in percentage is used to determine the accuracy [21]. A five percent (5%) error is set as the limit in this study [22]. The current sharing accuracy error percentage for 10%, 50%, and 100% loading conditions are shown in Figure 8. The current sharing accuracy error is highest during the 10% loading condition

and improves with increasing load because the increase in load current contributes to the sensed inductor current needed. Larger load translates to higher signal levels, thus, improving the current sharing capabilities.

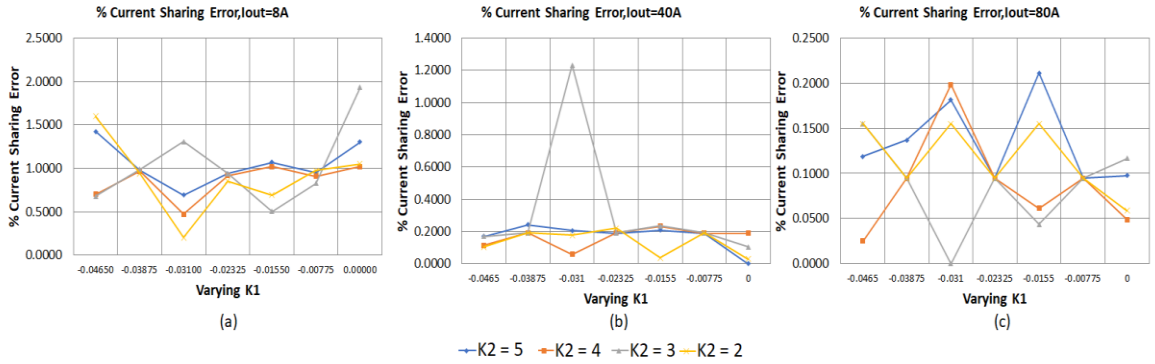


Figure 8. Current Sharing Accuracy Error for Different Control Gains at (a) 10%, (b) 50% and (c) 100% loading conditions.

Figure 9 shows the simulated waveforms during the load sharing of the two-phase VRM. The control gains for all instances are K_2 = 4 and K_1 = -0.031. At 10% load (Figure 9(a)), the output voltage, V_{out_sense}, is well within the regulation band. The inductor currents, i_1 and i_2, show that even with the very light load imposed on the VRM, they are dividing the load properly. Figure 9(b) illustrates the half load behavior of the VRM. As with the 10% loading condition, the converter is still within regulation and is also shared. Figure 9(c) shows the full load condition of the VRM. Again, the output voltage V_{out_sense} is regulating within the specifications. The inductor currents also exhibit an identical amount of load through each other. The load current voltage reference, $V_{\_iref}$, dictates the behavior of the inductor currents as this represents the amount of load presented to the converters.

It is also interesting to note that the behavior of the control gains cannot be deduced from the graph. Instead, what is noticeable is that all values of the control gains pass the current sharing error requirement. The choice of the control gains is then dictated mainly by other parameters.

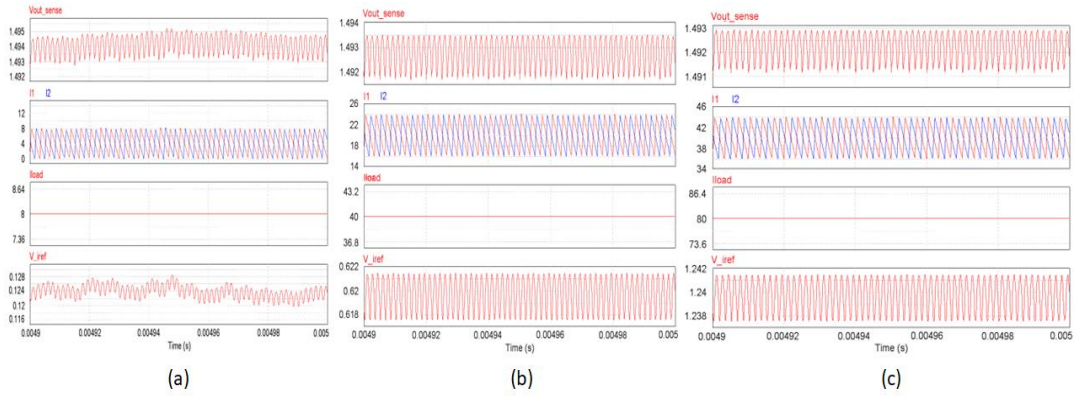


Figure 9. Operation of the VRM with *K2* = 4 and *K1* = -0.031 at (a) 8A, (b) 40A, and (c) at 80A load.

4.2. Dynamic Loading Conditions Results

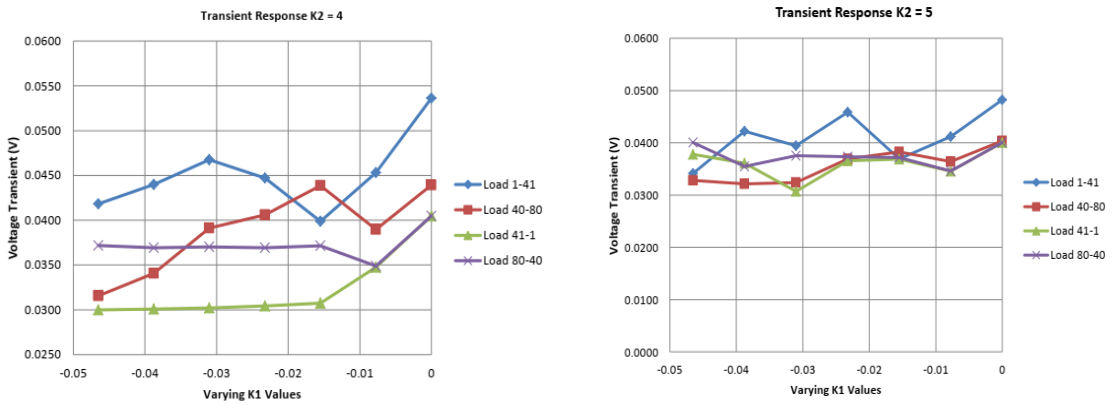
The two-phase VRM is also subjected to dynamic loading conditions for verifying the overshoot and undershoot requirements and the settling time of the converters. The control gains that resulted in the best response in the static loading condition simulation are used in the dynamic testing.

4.2.1. Transient Response

Figure 10 shows the transient response during dynamic loading at various control gains and loading conditions. During the lower-to-higher load transition, the undershoot decreases with more negative value of K_1. K_1 gives the feedback component due to capacitor current translating directly to *d/dt* of the output voltage. In the ideal case, the capacitor current would only vary with varying load (load transients). This component of the compensation is designed to counteract the *dV/dt* transitions of the output. Higher values translate to higher

"weights" given to this compensation parameter, thus, better undershoot performance. Examining the transition from higher load to lower load shows that the overshoot increases with increasing value of K_1.

For the two K_2 values presented above, the transient ripple only reached a maximum of ~55 mV at K_2 = 4 and ~50 mV at K_2 = 5. It is also observed that the variation of the undershoot from lower-to-higher load transition and the overshoot from higher-to-lower load transition is minimal. This makes SMC a better alternative for control.



(a) (b)

Figure 10. Transient Response Characteristics for Varying K_1 when (a) K_2=4, and (b) K_2 =5.

Figure 11 shows the dynamic loading response for one of the control gain settings. The output voltage and the inductor currents do not exhibit any oscillations. It is also observed that the inductor currents track each other perfectly well despite the disturbance at the load side, i.e., I1 waveform is equal to the I2 waveform.

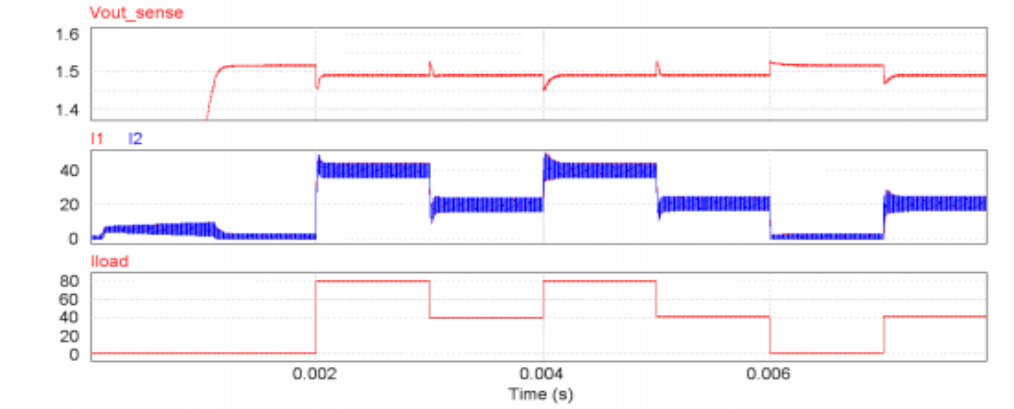


Figure 11. Dynamic Loading Condition K_2 = 4, K_1 = -0.031.

4.2.2. Beat Frequency Oscillation

The simulation model was subjected to varying load transient frequencies during the half load to full load transition to check if the control method is effective. The inductor current and output voltage are observed for oscillation and for sharing of the currents. Again, the best values used for the static loading condition are used in the test for the beat frequency oscillation. Table 2 to Table 4 show the response of the VRM with the application of load transient at varying frequencies. For all three high frequency load tests, the frequency of oscillation is obtained by observing the inductor phase currents. The oscillation is measured by adjusting the time scale and the voltage scale of the output waveforms in PSIM.

For all transient frequencies, the presence of beat frequency oscillation is still visible. In some cases, the beat frequency is twice the difference of the switching frequency and the load transient frequency. The "doubling" of the beat frequency is due to the phase shift present in the VRM. If the waveform is inspected closely, the actual frequency of beat is observed. The "doubling" is a result of the alternating power delivery to the load; thus, midway in the clock cycle of converter 1, converter 2 would provide energy as well. There are also instances when the beat frequency is no longer an integer multiple of the difference of the switching frequency and the load perturbation. This is due to the fast response of SMC that enables to track the signals immediately.

In summary, the following performance results have been obtained when employing the sliding mode control. First, the output voltage ripple is within the specified 15mV limit and the voltage regulation under loaded conditions is within the targeted 1.65% regulation band. Secondly, the two phases of the VRM can share the load within the defined 5% error limit. The dynamic performance shows sliding mode control as a very effective control method being able to handle the required 300mV transient ripple limit. Finally, the control is shown to greatly reduce beat frequency oscillations and no imbalance reaches more than twice the phase's capability.

However, choosing the control parameters is tedious due to the degree of freedom provided by the control equations, thus, it becomes necessary to characterize the behavior of each parameter and make compromises to achieve the desired performance. It has also been observed that the fast response produces undesirable double pulsing in the PWM and under certain conditions and control parameter values, the PWM may also exhibit cycle skipping.

Table 2. Beat Frequency Data for 290 kHz Load Transient Frequency

Control Gains		Output Voltage		Inductor Currents		Freq. of Osc (kHz)	Cycle Skip	Double Pulse
K1	*K2*	*Vout_max*	*Vout_min*	*I1_max*	*I2max*			
-0.0155	3	1.534	1.454	44.786	45.694	20	√	√
0	3	1.52	1.479	34.395	34.367	9.968		
-0.0465	4	1.606	1.55	40.796	40.631	20.246	√	√
-0.031	4	1.571	1.513	43.805	43.221	10.048	√	√
-0.0155	4	1.558	1.474	47.172	45.023	no specific freq	√	√
0	4	1.527	1.485	34.557	34.607	10		
-0.0155	5	1.586	1.46	53.71	54.678	no specific freq	√	√
0	5	1.538	1.463	43.959	42.848	no specific freq	√	√

Table 3. Beat Frequency Data for 300 kHz Load Transient Frequency

Control Gains		Output Voltage		Inductor Currents		Freq. of Osc (kHz)	Cycle Skip	Double Pulse
K1	*K2*	*Vout_max*	*Vout_min*	*I1_max*	*I2max*			
-0.0155	3	1.492	1.45	38.67	33.687	NONE	√	
0	3	1.52	1.483	34.1	34.006	NONE		
-0.0465	4	1.612	1.571	38.6	36.157	NONE	√	√
-0.031	4	1.579	1.579	35.578	35.652	NONE	√	√
-0.0155	4	1.51	1.469	38.545	33.681	NONE	√	
0	4	1.515	1.473	37.866	35.605	NONE	√	
-0.0155	5	1.572	1.469	51.959	50.584	19.08	√	√

5. CONCLUSION

In this paper, we have designed, derived and implemented a fixed frequency sliding mode controller applied to both the voltage control loop and the current sharing loop of the two-phase buck VRM for stability. The SMC-based controller has been evaluated on various extensive simulations with different types of load conditions. Results have shown that the SMC-controlled VRM is able to reduce the BFO phenomenon especially when the load transient is equal to the switching frequency. At 10 kHz from the switching frequency, the beat frequency is reduced to utmost 20 kHz. Also, the peak currents in the two phases of the VRM never exceeded twice its amplitude while maintaining a regulated output voltage within ±1.65% band.

It is advised to explore other state variables aside from those defined in the study. Some examples of the state variables that can be used instead of the ones defined are the derivatives of the voltage state variables. Also, it is recommended to implement reduction of state variables to reduce the computational complexities of the control.

Table 4. Beat Frequency Data for 310 kHz Load Transient Frequency

Control Gains		Output Voltage		Inductor Currents		Freq. of Osc (kHz)	Cycle Skip	Double Pulse
K1	*K2*	*Vout_max*	*Vout_min*	*I1_max*	*I2max*			
-0.0155	3	1.541	1.46	46.016	45.144	10.104	√	√
0	3	1.521	1.479	34.557	34.83	10.037		
-0.0465	4	1.606	1.55	40.235	38.473	10.101	√	√
-0.031	4	1.565	1.499	42.543	41.449	no specific freq	√	√
-0.0155	4	1.554	1.462	46.347	46.27	10.86	√	√
0	4	1.529	1.485	35.503	35.471	4.985		
-0.0155	5	1.565	1.472	47.791	47.741	17.694	√	√

0	5	1.537	1.464	41.97	41.771	10.274	√

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