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Multi-level swell voltage control for minimising damage to an on-grid system

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ABSTRACT

This article presented multi-level swell voltage control for minimising the damage to an on-grid system between 1.3 to 1.8 pu. in compliance with the value regulated by IEEE and IEC standards. A window comparator circuit and comparator circuit with hysteresis transistor were used as the voltage detector and excessive pulse entering the multi-level control of the load. According to the designed function at every stage in the form of fail-safe AND gate, the system was set for this case by turning to the fail-safe mode in order to prevent a fail-dangerous mode that might harm the electric system if the device in the detection circuit is deprived of a qualification that is against the condition. Due to the Failure Mode and Effect Analysis (FMEA) in accordance with IEC-6196-1, the function prevents electric and electronic devices in the on-grid system from incurring damage. The design and installation of the electric protection device SVSS have a parallel-connect with the electric system without concern for the load current.

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1. INTRODUCTION

In recent years, electronic technology has progressed consistently, becoming a major mechanism in the creation of many innovations including electric and electronic appliances, communication devices, and the smart on-grid power management network, which conforms to the State policy that encourages the development of the smart on-grid power network system in every region of the country in order to support the challenge of energy stability problems as well as global climate change. The installation of an on-grid solar power system [1-2] in a small house or rooftop PV system installation is a small-size electric generation system from 3-10 kw/household. Further, it conforms to the demands of users, as seen in Figure 1.

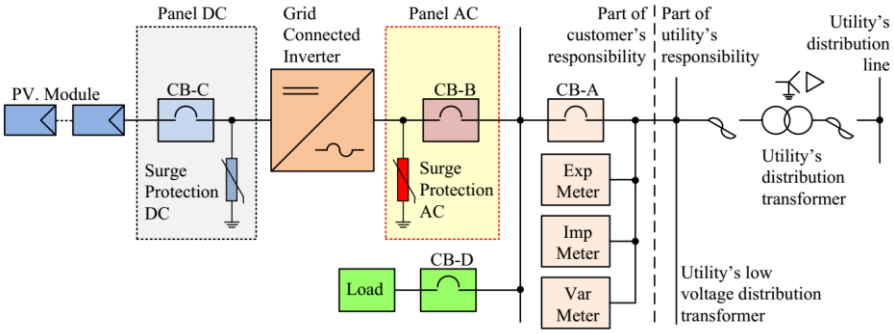

Figure 1. Pattern of the connection to the rooftop PV system

Electricity generated from the solar cell will be distributed to the grid-tie inverter for transforming DC electricity into AC electricity in the form of a sinewave, which shares the same frequency and voltage as the distribution system of the Electricity Authority. The generated electricity will be used through the loads

inside the residence, while the remaining electricity will be transferred to the Electricity Authority's system, which is connected to the electric network.

Quality problems concerning electricity [3] are frequently found in rural areas. Such problems stem from thunderbolts, capacitor bank switching, and the maintenance of the electric system, as well as the use of nonlinear devices, incorrect grounding, and the use of technology that does not agree with the electric system. These problems affect changes in electric quality. The installation of a protective device behind the meter remains limited to a Surge Protective Device (SPD) [4-8] or a Transient Voltage Surge Suppressor (TVSS) [9], which contains Metal-Oxide Varistor (MOV) for transient overvoltage only. When installing SPDs on AC Surge, the power electronic devices of the inverter will be damaged, as seen in Figure 2.

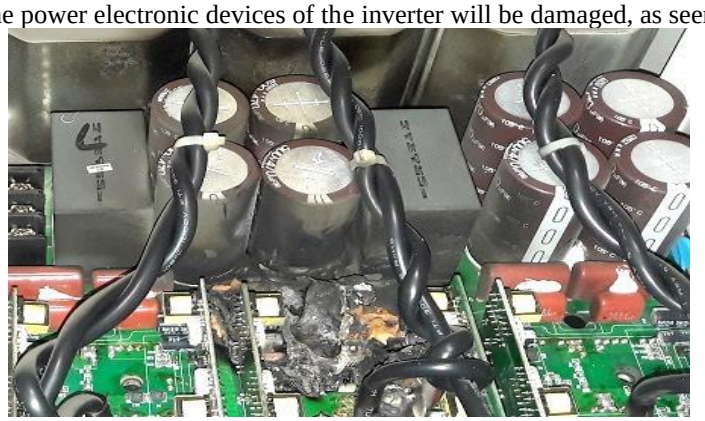

Figure 2. Damaged inverter from a change in electric quality

The damage to the inverter is impacted by the change of electric quality or voltage swell as the size of RMS voltage increases more than the criterion of IEEE Std 1159 and IEEE Std 1100 [10-11], as seen in Figure 3.

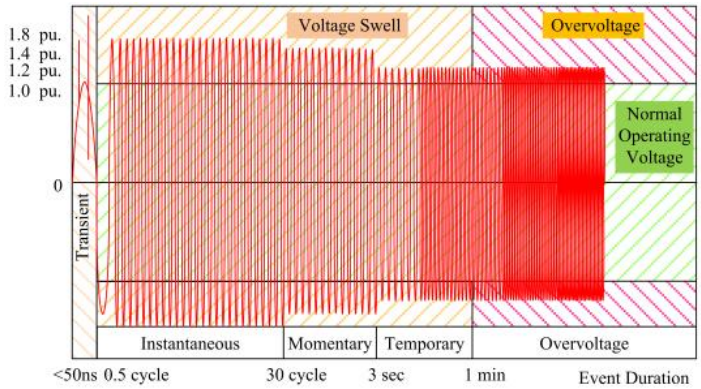

Figure 3. Voltage Reduction Standard of IEEE

The quality of electricity is regarded as a big problem for power electronic devices, which are sensitive. Impact reduction by using a Voltage Restorer (DVR) [12-13] as the transfer switch has the serial connection to the system, resulting in system stability. It requires the consideration of several factors because this solution is not appropriate for an on-grid system as the function of the inverter is not in accordance with the standard. It might cause danger to the user as well as the engineer who maintains the power system.

This article represents the concept to decrease the effect from the change of electric quality towards the electronic devices that connect to a solar cell that also connects to the electric network of the electricity authority. Problems arise from the voltage ripples RMS by SVSS (Swell Voltage Surge Suppression), which is used as a reducer of excess voltage with Surge Protection AC. Figure 1 shows the use of a window comparator circuit and a comparator circuit with hysteresis [14-17] to detect the surge overvoltage, which will process the data in analogue form in order to decrease the delay of MCU's working process for the fail-safe mode as well as to prevent harmonic impact. This could be further developed for commercial use.

2. RELATION MANAGEMENT FOR REDUCTION OF VOLTAGE OVERSURGE

Electric faults will cause surge overvoltage. If there is an abrupt change during <10 ms in the form of transient overvoltage, the MOV device for removing or absorbing the energy will reduce the surge overvoltage V_s, which is equal to V_{TVSS} in compliance with the IEEE Std 62.41 [7], as seen in Figure 4.

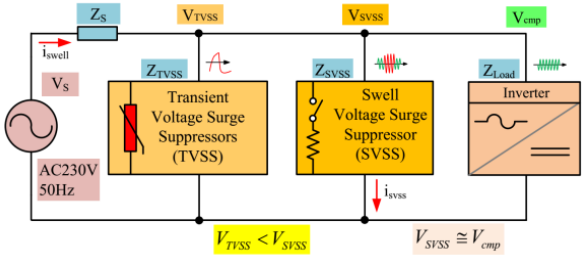

Figure 4. Relation Management for Reduction of Voltage Oversurge

After the swell voltage, the RMS voltage will increase over the standard limit, which is 10ms -1 min. The size is between 1.3 to 1.8 pu. It requires the use of a Swell Voltage Surge Suppressor (SVSS) that has been designed to install and connect in parallel with the electric system without as a mean tom remain the clamping voltage (V_{cmp}) at V_{SVSS}, which is the level that prevents failure in power electronic devices. When the overvoltage cannot access the work of TVSS, it results in Z_{TVSS} high impedance and clamping voltage. SVSS and the inverter share a similar value as that for equations (1), (2), and (3).

$$V_{TVSS} < V_{SVSS} \cong V_{cmp} \quad (1)$$

$$V_{SVSS} = \frac{Z_{SVSS}}{Z_S + Z_{SVSS}} \times V_S \quad (2)$$

$$i_{swell} = \frac{V_S}{Z_S + Z_{SVSS}} \quad (3)$$

3. DESIGN OF VOLTAGE SWELL DETECTOR

The Voltage Swell Detector is the circuit that detects the crest of overvoltage. The output signal will control the load, letting the voltage through the load at 230V±10% in accordance with the IEEE Std 1159 and IEEE Std 1100. The Voltage Swell Detector will use the high voltage transistor with V_{CE} at 300 V following the parameter of KSP42 and KSP92 in order to endure the disturbing signal and overvoltage. The detector consists of Window Comparator Multi-Stage (WCS) that scopes the range of multi-levelled output voltage and Comparison with Hysteresis (CH) that detects the hysteresis voltage and pulse. The design for the starting level of voltage must conform to the function of the inverter such as the inverter Growatt 3.6 kW works at 180-280 V or 0.8-1.2 pu.

The relationship of multi-level minimising voltage by designing the voltage swell detector V_s to have multi-levels, which are WCS-1, WCS-2, WCS-3,…, WCS-n, between 1.3 to 1.8 pu. or +30-80% to prevent the effect of the inverter. The working process of the window comparator can be divided into 3 levels including Stage 1, Stage 2, and Stage 3. The different stages work differently. Stage 1 has WCS-1 dealing with the overvoltage at 1.3-1.4 pu. or +30-40%, while Stage 2 has WCS-2 dealing with the overvoltage at 1.5-1.6 pu. or +50-60%. Finally, Stage 3 has WCS-23 dealing with the overvoltage at 1.7-1.8 pu. or +70-80%. When V_{dc_in} increases to the level of set voltage, the output signal V_{o_WCS-1}, V_{o_WCS-2} and V_{o_WCS-3} will be released, as illustrated in Figure 5.

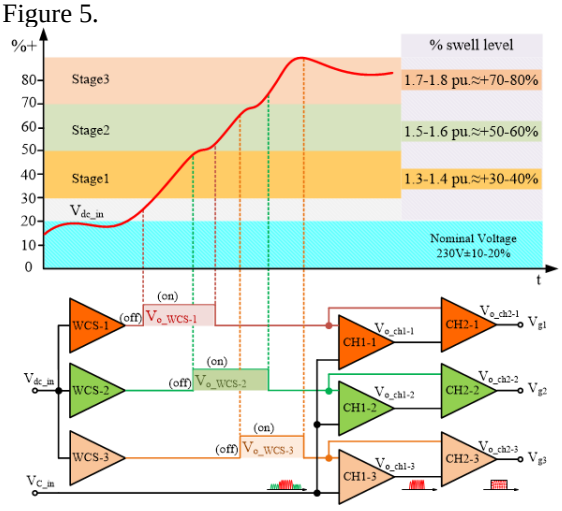

Figure 5. Voltage Swell Detector

3.1. The window comparator circuit with transistor

The design of a voltage swell detector usually uses a window comparator. In general, people often apply the IC Op-amp or IC Module [18-20], which is appropriate for analysing small-size signals and uses a low-voltage source. Adaptation for the voltage swell detection still has a limit. The design of the window comparator requires 4 transistors for each set [14-15], which will work separately with Q_1 and Q_2 working as the oscillator, while Q_3 and Q_4 work as the amplifier. The setting of output signal V_o can set the window at 2 levels, including High Voltage (V_H) and Resistor R_1 and R_2. For Low Voltage (V_L), there are Resistor R_3 and R_4, as seen in equations (4) and (5).

$$V_L = \left(\frac{R_2}{R_1 + R_2}\right) \times V_{CC} \tag{4}$$

$$V_H = \left(\frac{R_4}{R_3 + R_4}\right) \times V_{dc\_in} \tag{5}$$

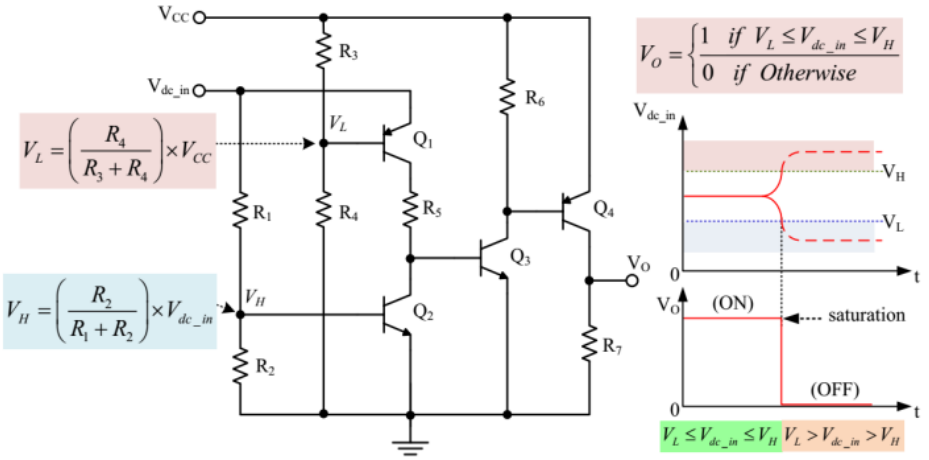

Figure 6. Window Comparator with Transistor and Output Signal

From Figure 6, which demonstrates the characteristics of the output signal of the window comparator circuit, the output signal will maintain its status as 1 or ON if the voltage V_{dc_in} is inside window V_L and V_H, as seen in equation (6).

$$V_L \le V_{dc\_in} \le V_H \tag{6}$$

When V_{dc_in} departs from window V_L and V_H, the output signal will maintain its status as 0 or OFF, as seen in equation (7).

$$V_L > V_{dc\_in} > V_H \tag{7}$$

Otherwise, the output signal V_o will be as seen in equation (8).

$$V_{CC}\left(\frac{R_4}{R_3 + R_4}\right) \le V_{dc\_in} \le \left(\frac{R_2}{R_1 + R_2}\right) V_{dc\_in} \tag{8}$$

Failure Modes and Effects Analysis (FMEA) [21-23], along with the window comparator circuit, will be the indicator of fail-safe analysis for voltage swell detection. It could be adapted to prevent damage. The principle of analysis has been regulated in the standard and the result from the analysis will confirm that the window comparator circuit will work in fail-safe mode. If any fail-dangerous mode occurs with any window comparator or all three sets, the switch load will stop working immediately and the window comparator will not cause fail-dangerous to the system, as seen in Table 1.

Table 1. Result of Failure Modes and Effects Analysis (FMEA) of the created Window Comparator Circuit

Devices	Failure Mode	Effect of the Window Comparator	Effect of Failure	Effect of Switch Load
R_1	Open circuit	Change of circuit characteristic	d	Δ
	Short circuit	Change of circuit characteristic	d	
	R_1* 2	Change of circuit characteristic	d	
	R_1* 0.5	No output signal	b	
R_2	Open circuit	Change of circuit characteristic	e	Δ
	Short circuit	No output signal	d	
	R_2* 2	No output signal	d	
	R_2* 0.5	Change of circuit characteristic	d	
Q_3	Open circuit	No Output Signal	b	Δ
	Short circuit	No Output Signal	b	

Notes: (* 0.5) and (*2) are in reference to the standard measurement
(a): Normal Output l (b): No Output (c): window Voltage reduced (d): window Voltage increase
(e): Output as V_{cc} (f): Half reduction output
Δ : No significant consequences of Switch Load

3.2. Comparison with Hysteresis

Comparison with Hysteresis (CH) detects the hysteresis signal, working similarly to the window comparator. Hysteresis [14-15] occurs from some amount of output high voltage reversing the input signal. It examines the width of the pulse signal, which enters the system excessively. It is the adaptation of hysteresis in the use of frequency counter [24] and removes the swing of the input signal that enters to minimise the failure, as seen in Figure 7.

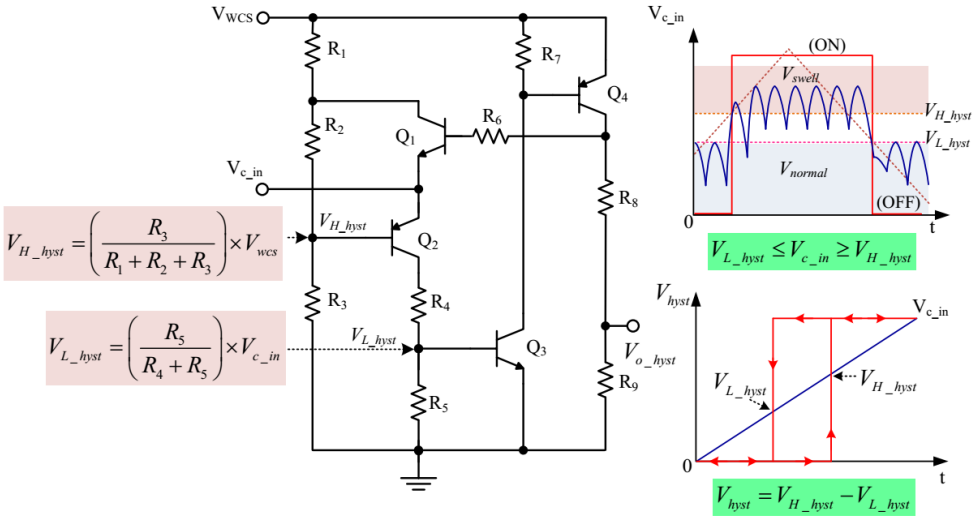

Figure 7. Comparison with Hysteresis and Output Signal

From Figure 7, the design of comparison with hysteresis employs 4 transistors per set. Q_1 works as the reverse circuit of the output signal, while Q_s and Q_3 work as the oscillators and Q_4 works as the amplifier. The setting of the output signal V_{hyst} could start from V_{H_hyst} and replace resistors R_1, R_2, and R_3. The voltage starts to change to low voltage V_{L_hyst}, meaning the resistors can be replaced by R_4 and R_5.

If V_{c_in} between V_{H_hyst} and V_{L_hyst}, the output signal V_{o_hyst} will be 1 or ON, as seen in Figure 7. When V_{c_in} departs from the aforementioned condition, the output signal will be 0 or OFF, as seen in equation (9).

$$V_{L\_hyst} \le V_{c\_in} \ge V_{H\_hyst} \quad (9)$$

To find the hysteresis voltage V_{hyst}, see equations (10), (11), and (12).

$$V_{hyst} = V_{H\_hyst} - V_{L\_hyst} \quad (10)$$

$$V_{H\_hyst} = \left(\frac{R_3}{R_1 + R_2 + R_3} \right) \times V_{wcs} \quad (11)$$

$$V_{L\_hyst} = \left(\frac{R_5}{R_4 + R_5} \right) \times V_{C\_in} \quad (12)$$

After performing Failure Modes and Effects Analysis (FMEA) of Comparison with Hysteresis, the analysis of fail-safe is used to detect overvoltage as well as prevent damage.

3.3. Bridge Rectifier

The bridge rectifier receives direct energy from the input voltage V_s that enters the system in the form of an AC sine wave and transforms to DC voltage V_{dc}. Regarding the calculation to find the highest voltage in accordance with the level of swell voltage with % swell, see equation (13).

$$V_m = \frac{\sqrt{2} \times 230 \times \%swell}{100} \quad (13)$$

Regarding the calculation to find the highest DC voltage in accordance with the level of swell voltage with % swell, see equation (14).

$$V_{dc} = \frac{\frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t d\omega t \times \%swell}{100} \quad (14)$$

The highest voltage flows to the voltage divider circuit, in which 2 loads resist the serial circuits. To find the clamping voltage (V_d) of R_2, as seen in Figure 8, see equation (15).

$$V_d = V_{dc} \times \frac{R_2}{R_1 + R_2} \quad (15)$$

3.4. Low Pass Filter

The design of the Low Pass Filter (LPF) is intended to eliminate ripple voltage (V_r). It maintains the components of direct current. To find the RMS of ripple voltage V_r (RMS) and DC Voltage V_{dc_in}, see equation (16).

$$V_{dc\_in} = V_m - \frac{I_{dc}}{4 \times f \times C} \quad (16)$$

3.5. RC Integrator (RCI)

The design of RC integrator is intended to adjust the integrated wave and analyse the RC integrator, whose value is stable. For the clamping voltage of the capacitor (V_{c_in}) during charging, see equation (17).

$$V_{C\_in} = V_d (1 - \varepsilon^{-t/RC}) \quad (17)$$

For the clamping voltage of the capacitor during discharge, see equation (18).

$$V_{C\_in} = V_d \varepsilon^{-t/RC} \quad (18)$$

V_{dc_in} increases in window V_H and V_L. With regard to the setting of the function of WSC, the output signal V_{o_WCS} will be ON. Apart from this condition, it will be OFF and the output signal will be out of WSC and send the signal to CH2 to join the output signal CH1. It forms an AND gate, as seen in Figure 8.

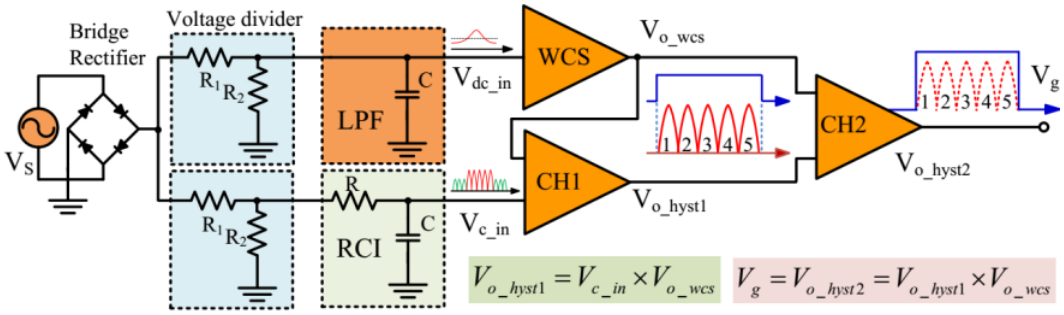

Figure 8. Voltage Swell Detector of all stages in the form of AND gate

When voltage V_{c_in} has a value in compliance with CH1's function, which is the circuit that detects the frequency and the level of voltage at the same stage WCS, it will signal V_{o_hyst1} to come out in the number of pulses for input V_{C_in} that excessively come in. Passing the CH2 circuit to be with signal V_{o_wcs}, the output signal of CH2 is equal to V_{o_hyst2} and the status is 1 or ON according to the logic of AND gate. Apart from this condition, the output signal will be 0 or OFF, as seen in equations (19) and (20).

$$V_{o\_hyst1} = V_{c\_in} \times V_{o\_wcs} \quad (19)$$

$$V_g = V_{o\_hyst2} = V_{o\_hyst1} \times V_{o\_wcs} \quad (20)$$

3.6. 3-Level Load Control

Block diagram for 3-level load control [25], which examines the level of overvoltage between 1.3 to 1.8 pu. Stage1 has WCS-1, Ch1-1, and CH2-1 to cope with the transient overvoltage between 1.3 to 1.4 pu. Stage2 has WCS-2,Ch1-2,and CH2-2 to cope with the transient overvoltage between 1.5 to 1.6 pu.Stage3 has WCS-3, Ch1-3, and CH2-3 to cope with the transient overvoltage between 1.7 to 1.8 pu, as seen in Figure 9.

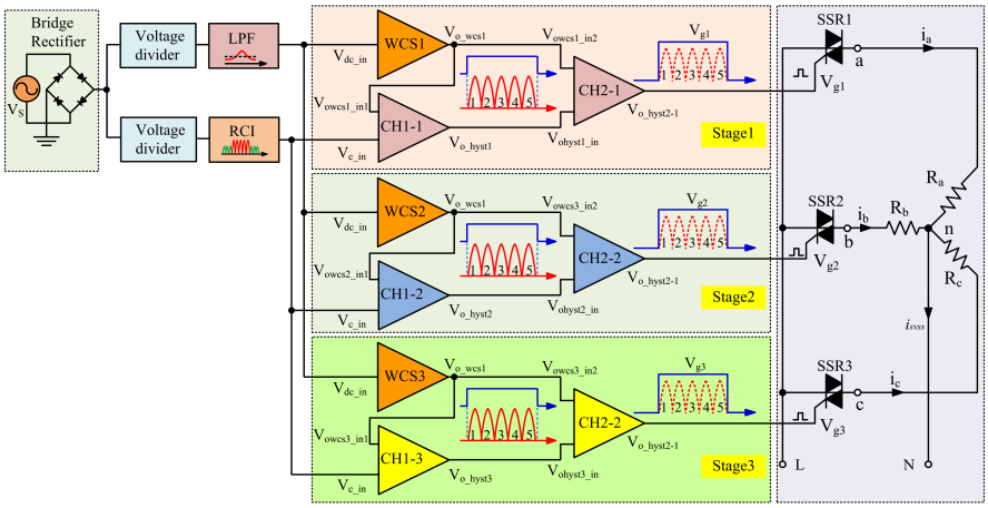

Figure 9. Block Diagram of 3-Level Load Control

From Figure 9, the transient voltage of the single-phase is set using equations (21) and (22).

$$i_{swell} = i_{svss} = \frac{V_S}{Z_S + Z_{SVSS}} \quad (21)$$

$$V_{SVSS} = i_{swell} Z_{SVSS} = \frac{Z_{SVSS}}{Z_S + Z_{SVSS}} V_S \quad (22)$$

The window of every stage has a time delay to prevent transient ripple voltage, as seen in Figure 10.

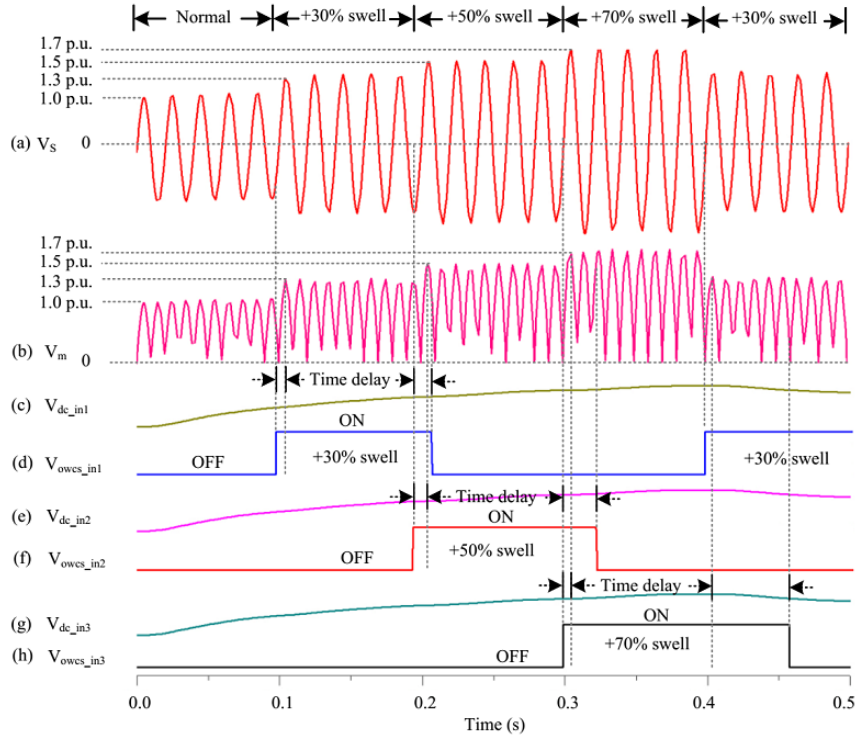

Figure 10. Simulation Result for 3-stage Voltage Swell Detection of the Window Comparator

It detects the transient overvoltage of every stage in the form of AND gate, resulting in better efficiency for the control of each load. The simulation sample of the output signal of the control in Stage 2 that distributes +50% voltage swell for 100 ms is presented in Figure 11.

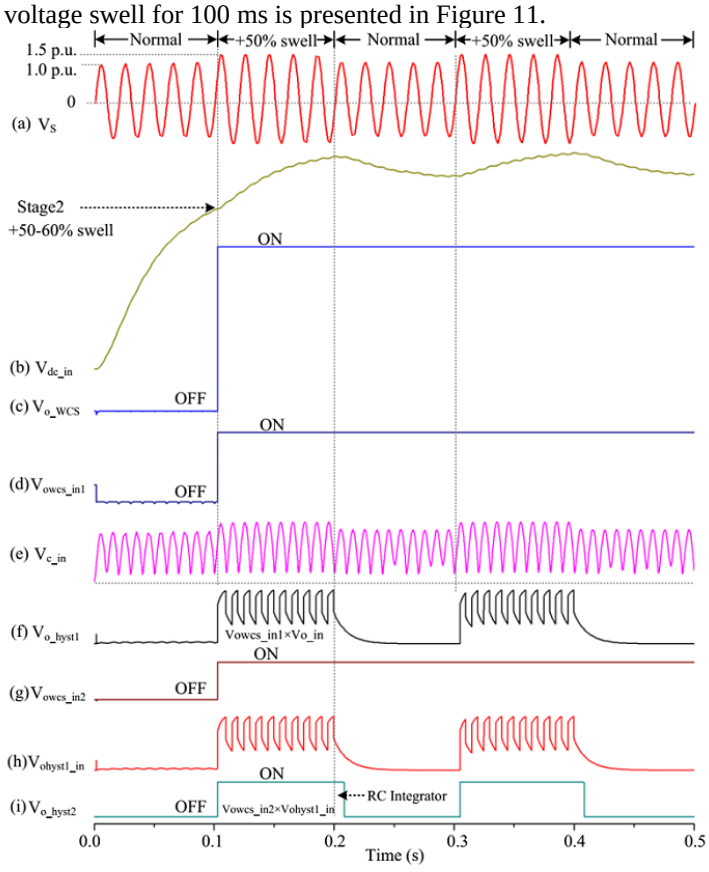

Figure 11. Result from the Simulation of Control Signal for Voltage Swell Detection at Stage 2

The output signal used for driving the Solid State Relay (SSR) of Stage 1 V_{g1}, Stage2 = V_{g2}, and Stage3 = V_{g3} to control the load with a resistor of loads is as follows: R_a, R_b, and R_c having the consistency with overvoltage. This is an easy solution and uses the least resistor load.

In the normal state, V_{g1} = 0, and electricity i_a = 0, when voltage swell between 1.3 to 1.4 pu. enters SVSS. The output at Stage 1 will be ON and V_{g1} = 1, resulting in SSR1 turning off. The electricity I_{SVSS} flows through resistor Ra, causing the clamping voltage at an, as seen in equation (23).

$$V_{SVSS\_stage1} = V_{an} = i_a \times R_a \tag{23}$$

When voltage swell between 1.5 to 1.6 pu. enters SVSS, the output at Stage 2 will be ON and V_{g2} = 1, resulting in SSR2 turning off. The electricity I_b flows through resistor R_b, causing the clamping voltage at bn, as seen in equation (24).

$$V_{SVSS\_stage2} = V_{bn} = i_b \times R_b \tag{24}$$

When voltage swell between 1.7 to 1.8 pu. enters SVSS, the output at Stage 3 will be ON and V_{g3} = 1, resulting in SSR3 turning off. The electricity I_c flows through resistor R_c, causing the clamping voltage at cn, as seen in equation (25).

$$V_{SVSS\_stage3} = V_{cn} = i_c \times R_c \tag{25}$$

The voltage from voltage swell at % (swell) is found using equation (26).

$$V_{swell} = \frac{V_{s\_normal} \times \%swell}{100} \tag{26}$$

To find the power of load or resistor power P_r and the clamping voltage V_{cmp} of the control load in every stage, equations (27) and (28) are used.

$$P_{r\_stage} = I_{svss}^2 \times R_{stage} \tag{27}$$

$$V_{cmp} = I_{svss} \times R_{stage} \tag{28}$$

4. EXPERIMENT OF MULTI-LEVEL SWELL VOLTAGE

The installation of swell voltage protection in the rooftop PV system is a protective measure to reduce the risk that might occur from the failure of electric and electronic devices. The experiment of the control load for minimising the overvoltage will connect parallel to the low voltage electrical system [26-30], in which the meter is type 1, phase 230 V, 5A. The voltage over the standard is distributed at +30-80%, or 299-404V, and the clamping voltage is measured at the protective device V_{SVSS} or V_{cmp}, which is sensitive to the load, as seen in Figure 12.

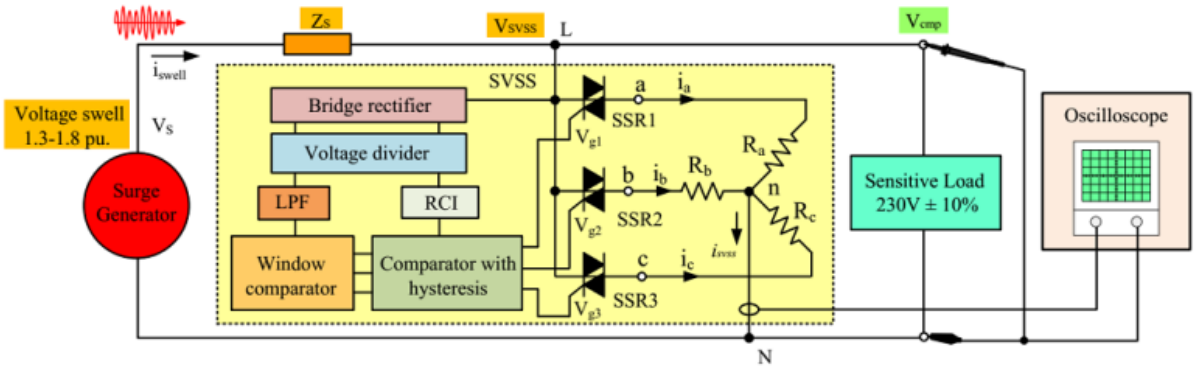

Figure 12. Experiment of Multi-Level Swell Voltage

Figure 13. Experiment of Multi-Level Swell Voltage

Figure 13 demonstrates the experiment of multi-level swell voltage. When the voltage reached the destined level, the output signal through the windows V_{g1}, V_{g2}, and V_{g3} to control the loads in accordance with the overvoltage. as seen in Figure 14.

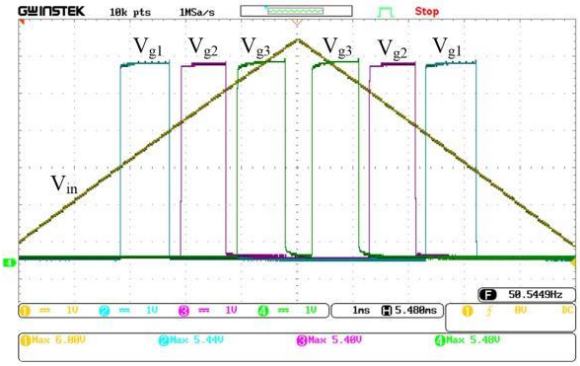

Figure 14. Input and Output Signals of multi-stage window comparator for SVSS control

Distribute the swell voltage at +30-80% at 50 Hz, then use the oscilloscope to measure the size of the wave, as seen in Figure 15, respectively. The results are recorded in Table 2.

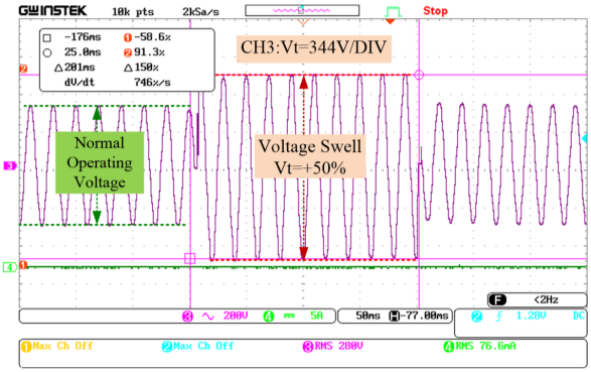

Figure 15. Wave of Voltage Swell at +70%

Table 2. Record of the Experiment for Control Load to Minimise Swell Voltage

Sequence Test	+% Swell [%]	Voltage test Vt[V]	Clamping voltage Vcmp[V]	Leakage current Cl[A]	Power Resistor Pr[W]
1	30	299	237	1.57	372.09
2	40	320	231	2.38	549.78
3	50	344	248	2.56	634.88
4	60	366	211	4.34	915.74
5	70	386	224	4.85	1,086.4
6	80	406	236	5.22	1,231.92

Multiple test results for transient voltage control circuits can detect the voltage as designed. The created window circuit compared to the operation with the simulation circuit obtained results demonstrating that the voltage level can be detected. From the equation 26, 27, and 28. That is, voltage level (V_t) 299V – 320V Stage1 will work, causing the electric current (Cl) to flow through the load 1.57A - 2.38A, producing force. The voltage drop (V_{cmp}) across the load 237V - 231V at voltage level (V_t) 344V - 366V Stage2 will work, causing the electric current (C_l) to flow through the load 2.56A - 4.34A, causing the voltage drop (V_{cmp}). The load bracket 248V - 211V and at voltage level (V_t) 386V - 406V Stage3 will work, causing electricity (Cl) to flow through the load 4.85A - 5.22A, causing voltage drop (V_{cmp}) across the load 224V - 236V to control the overvoltage of the transient not exceeding the standard value by a control circuit that does not cause damage due to the analysis of damage characteristics and potential impact (FMEA) before the real test.

Table 2 demonstrates the oscilloscope of the clamping voltage V_{cmp} and electric current I_{svss} flowing through SVSS of swell voltage at these sizes in Figures 16, 17, and 18, respectively.

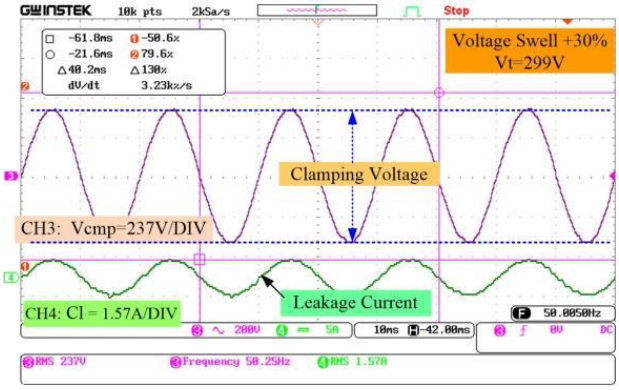

Figure 16. Expansion of Wave of Voltage Swell at +30% and Electric Current Through SVSS at Stage1_ON

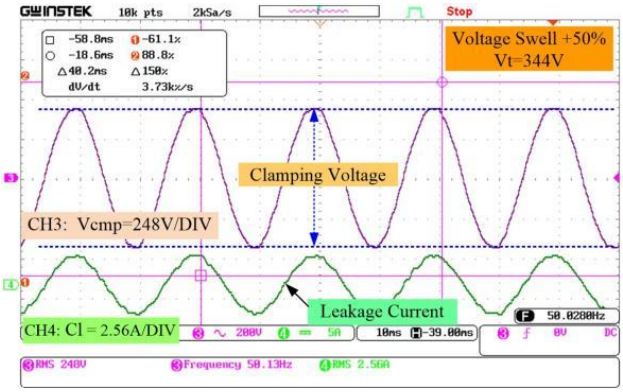

Figure 17. Expansion of Wave of Voltage Swell at +50% and Electric Current Through SVSS at Stage2_ON

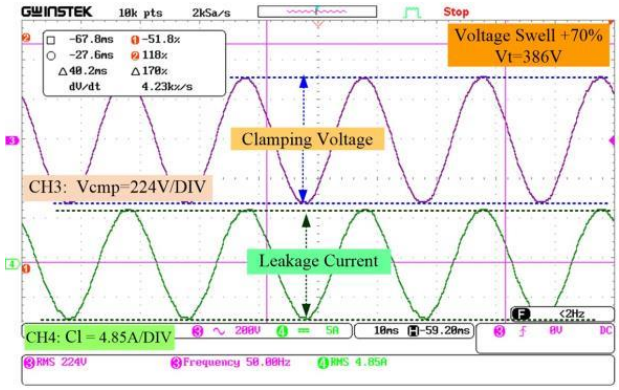

Figure 18. Expansion of Wave of Voltage Swell at +70% and Electric Current Through SVSS at Stage3_ON

Performance measurement of multiple levels of transient over-voltage regulation in the characteristics of the test voltage and the voltage across the load from Figure 16 presents the operation of

SVSS at Stage 1. Figure 17 shows the operation of SVSS at Stage 2, while Figure 18 shows the operation of SVSS at Stage 3. The SVSS device can be used as a strengthening material and can overpressure electricity due to the same behavior as the TVSS devices in the form of clamping voltage; when the overvoltage goes into the on-grid system with the voltage level of the SVSS device, the SVSS device will have the load switch (ON) accordingly. The excess voltage level in the system causes the SVSS device to return to a low impedance value, resulting in the momentary flow of electric current through the load. When the voltage in the system has returned to normal, the SVSS device will stop working (OFF), causing the SVSS device to return to the same high impedance value, etc. Measuring the output of the SVSS device will find that the waveform of voltage and current are not distorted from the original, preventing harmonics from occurring in the system. The installation of SVSS equipment will be carried out in parallel with the electrical system, which is suitable for the on-grid system.

Table 2 demonstrates the result in the graph of the relationship between voltage, electric current, and electric power of the minimising swell voltage set, as seen in Figures 19, 20, and 21, respectively.

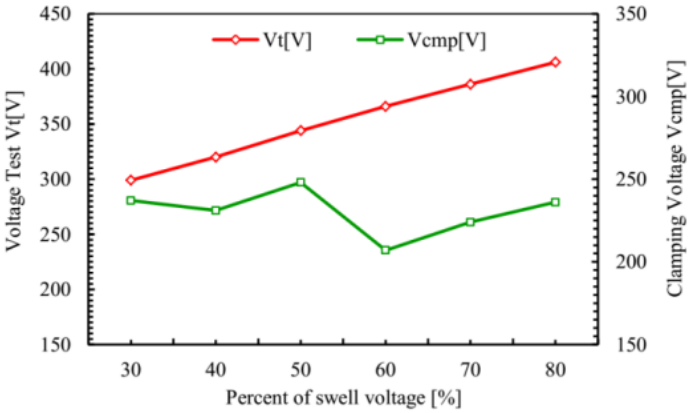

Figure 19. Relationship between Testing Voltage and Clamping Voltage at %Swell

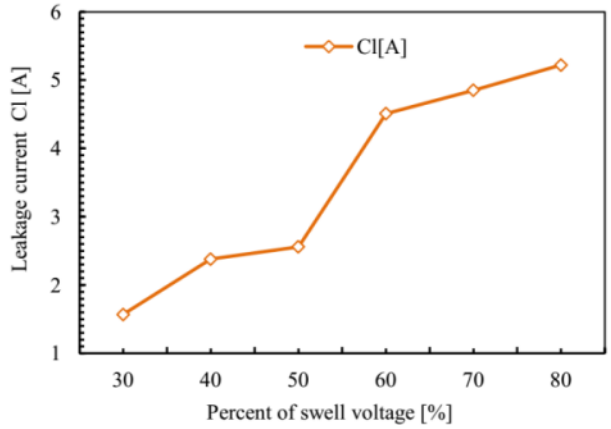

Figure 20. Relationship of Electric Current through SVSS at %Swell

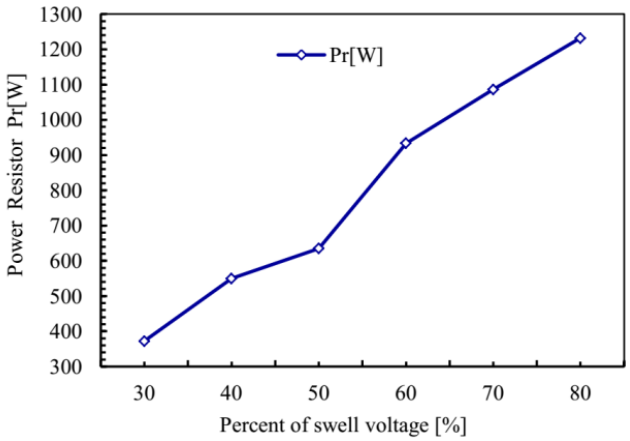

Figure 21. Relationship of Transient Load Capacity at %Swell

5. CONCLUSION

This article demonstrates the multi-level swell voltage control for minimising damage to the on-grid system that connects the electric power of the electricity authority with 3-stage swell voltage control. Every stage contains a window comparator and comparison with hysteresis as the controllers and counting the extra pulse signal. It controls the load as designed for the function of every stage in the form of AND gate, which is complicated. If one of the circuits is deprived of qualification or runs against the condition, the system will abruptly turn to the fail-safe mode in order to prevent a fail-dangerous condition in the system. Based on Failure Modes and Effects Analysis (FMEA) of the aforementioned window comparator, the result is in accordance with the IEC 61496-1 as the details for every stage to examine failure have been indicated. Swell voltage control between 1.3 to 1.8 pu. can minimise the voltage, not over the IEEE and IEC standard, in which the dangerous effect is that the device becomes sensitive. This method makes the system sensitive to having a protective response to prevent damage.

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