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Design of the Digital I/O Pad Buffer for Mixed-Voltage Application

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ABSTRACT

A new circuit design of digital bidirectional input/output (I/O) pad buffer for mixed voltage is presented. The digictal bidirectional I/0 buffer is designed to avoid reflections by matching the output impedance to the 50 ohms of the transmission line and having overshoots and undershoots below 300mV by increasing the output impedance. The digital bidirectional I/O pad buffer provides minimum delays between input and output and minimum rising and falling times. The proposed digital bidirectional I/O pad buffer was designed, simulated and layouted in Cadence using in TSMC 0.18um CMOS process with a linear resistive element electrically connected at an I/O pad for limiting a processed data I/O signal. The output rising time and falling time are 0.42 ns and 0.93 ns with 3pF load respectively. The final chip area is only 5 um^2

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1. INTRODUCTION

To reduce the silicon cost, to increase circuit performance and high speed operating. The dimension of transistors has been scaled down towards the nanometer region, and the power supply voltage has also decreased [1]. However, it is hard for system design to convert all high voltage components into low voltage integrated circuits due to the cost consideration. Therefore, many microelectronic systems often require internal integrated circuit components to be designed with a mixed-voltage interface [2]. For example, a chip that operates with 1.8V internal power supply voltage may receive signals of 3.3V from external components, so you have to design mixed-voltage I/O buffers for the 1.8V chip. Although mixed-voltage I/O buffers have overcome several problems, such as gate-to-oxide reliability [3], due to the high electric field resulting from the high voltage difference between the gate-drain and gate-source terminals, degradation of hot carriers [4], occurs when the drain-source voltage of the transistor operating in saturation mode is greater than the normal operating voltage. Undesired circuit leakage paths [5] occur from the I/O pad to the power supply voltage through this parasitic PN-Junction diode.

To overcome these problems, several mixed voltage I / O buffers have been proposed. To avoid the problem of the reliability of oxide carriers, a mixed voltage I / O buffer with an NMOS blocking technique has been proposed [6]. But, operating in the ultra-low voltage region, the use of these techniques can limit the voltage oscillation of the received inputs, degrading the reception speed. In [7], special polarization techniques can be used to prevent degradation of hot carriers. To eliminate unwanted circuit leakage paths, a mixed voltage I/O buffer adopting gate voltage tracking and dynamic n-well bias techniques has been proposed [8]. However, the buffer requires many additional transistors having complicated connections, resulting in increased design cost and area of layout. In this article, a new digital I/O buffer circuit design is proposed to provide a small area, to avoid reflections, minimum delays between input and output, minimum rise and fall times, and overshoots and undershoots of less than 300 mV.

2. PROPOSED DIGITAL I/O PAD BUFFER

The block diagram of the proposed digital I/O pad buffer is shown in Figure 1. The output stage is the same for the two digital I/O pad buffers.

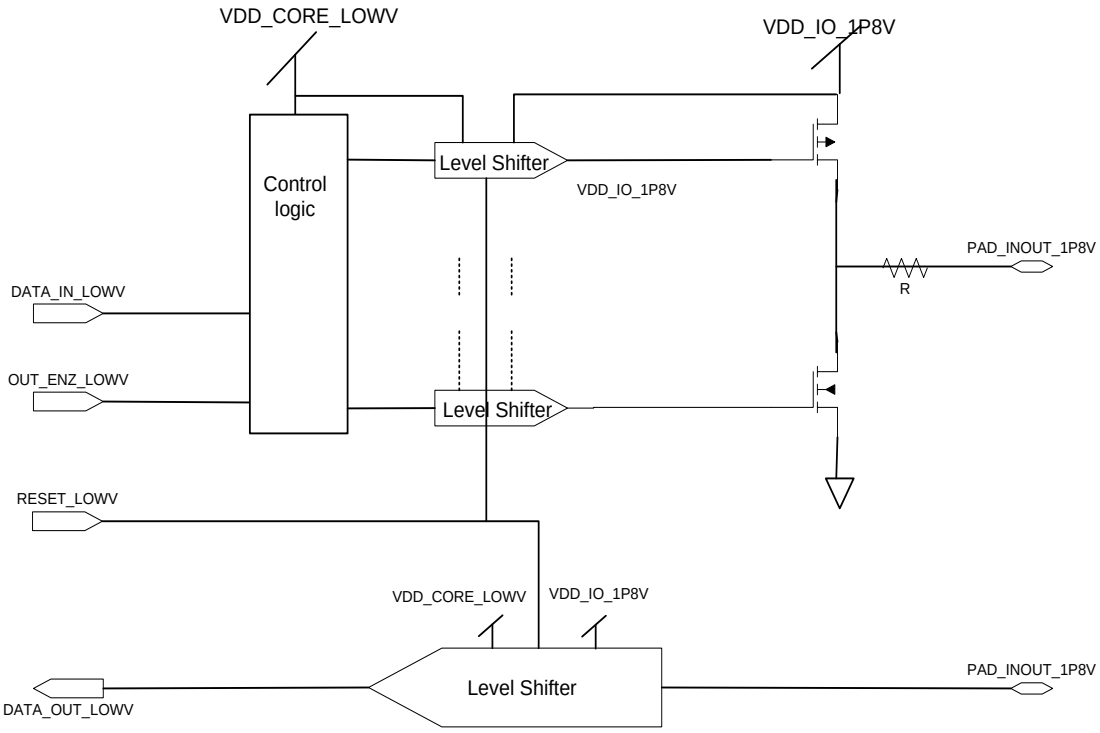

Figure 1. The block diagram of the proposed Digital I/O pad buffer

The proposed digital I/O pad buffer consists of two parts; input part and output part. The input part is composed of a schmitt trigger and inverter control logic. The output part comprises a logic control, a PMOS driver, a NMOS driver, an output stage and a linear resistive element electrically connected at an I/O pad for limiting a processed data I/O signal. The digital I/O buffer controls I/O output impedance using a combination of FET pull-up and pull-down in series with a linear resistive element. The pull-up and pull-down stages include the respective PMOS driver and NMOS driver, which are controlled by a logical circuit.

The logical control utilizes these signals to generate logical signals to control the PMOS driver and NMOS driver. The PMOS driver and NMOS driver, therefore, control the output stage. It is this controlled active output impedance in series with a fixed linear resistive element.

The linear resistive R may be configured to provide a significant portion of the pad output impedance.

The trade-off to design the output impedance of the buffer:

- To have an output impedance as close as possible to the 50 ohms of the transmission line, avoid reflections.
- To be large enough to minimize the delays between input and output are requested, need to reduce the output impedance
- To have overshoots and undershoots below 300mV, need to increase the output impedance
- To have relative small rising and falling times, need to reduce the output impedance

The proposed design concept of digital bidirectional I/O buffer is shown in Figure 2. The design was carried out according to the following priority; Increase the output impedance as much as possible by reducing the size of the PMOS and NMOS output to meet the specification of input to output delay, and to meet the specification of rise and fall times, and to obtain a higher output impedance and as close as possible to 50 ohms. And check that the overshoots and undershoots do not exceed 300mV.

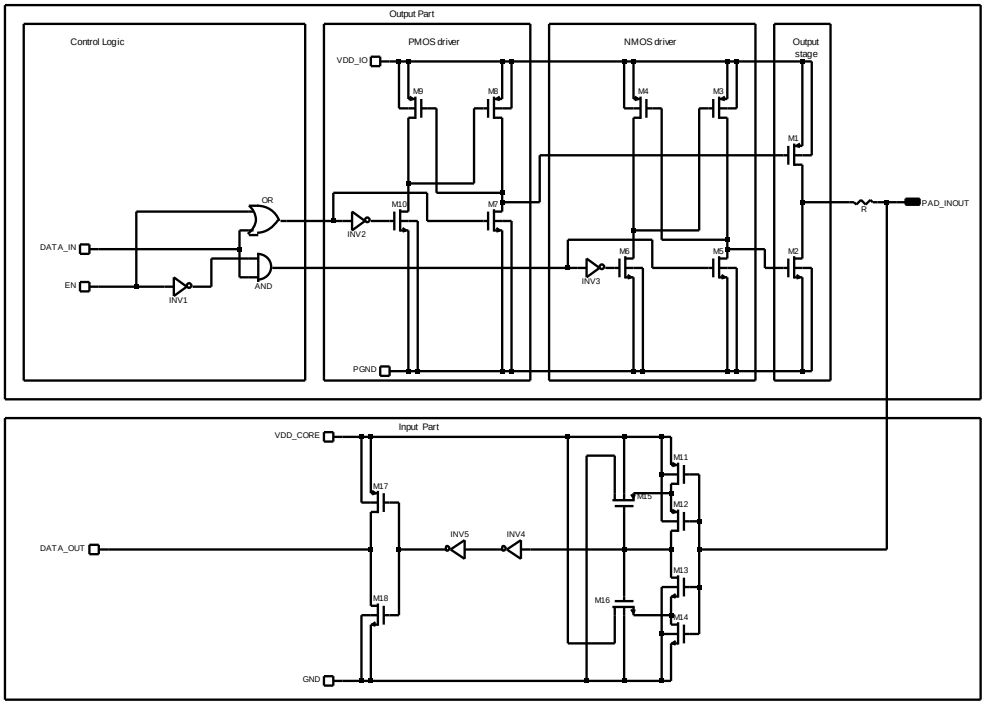

Figure 2. The proposed design concept of digital bidirectional I/O buffer

3. SIMULATION AND RESULTS

The design of the digital I/O pad buffer has been implemented in TSMC 180 nm CMOS technology. The digital pad buffer is characterized using ACS with:

- Statistical Models (No Matching)
- Corner Models (Nmos= weak or strong, Pmos= weak or strong)

The electrical simulations for the output stage take into account:

- Layout parameters
- ESD structure used
- Package Models
- Lines specifications.

As shown in Figure 3, the following block diagram gives the test bench to be used for electrical simulations:

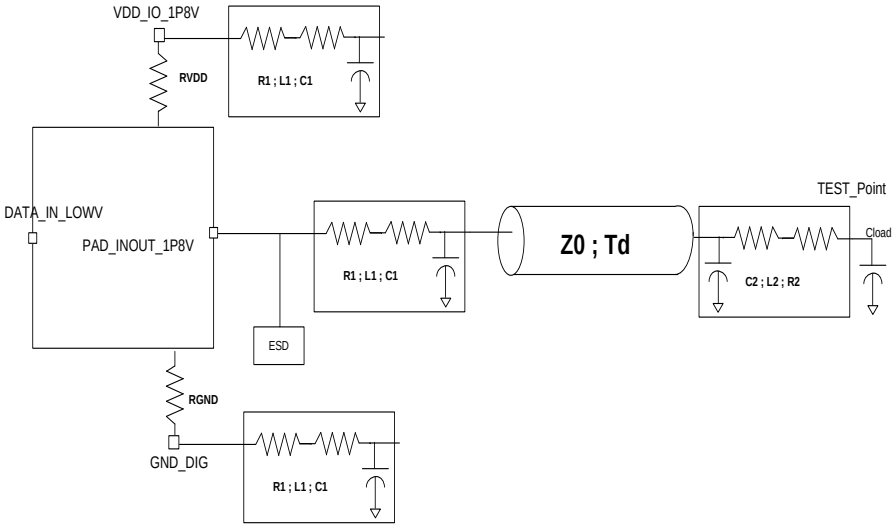

Figure.3. Block diagram for electrical simulations

3.1. Layout of the Digital I/O pad buffer proposed

The layout and extracted of the proposed digital I/O pad buffer are shown in Figures 4 and 5. All devices or circuits prone to produce electromagnetic interference or susceptible to interference are enclosed with double-layer guard rings. The layout is done by respecting the following items; design rules (DRM, MRC, and Density) and designer constraints information (constraint manager, matchCat…) and use only metal1, metal2, and Metal-6 layer are not used. We choose the coupled model for the extracted (Assura RCX, R-C model) because it gives worst results than the de-coupled (reference=GND_DIG) model. The total area of the proposed circuit in TSMC 180 nm technology is 0.005 mm^2.

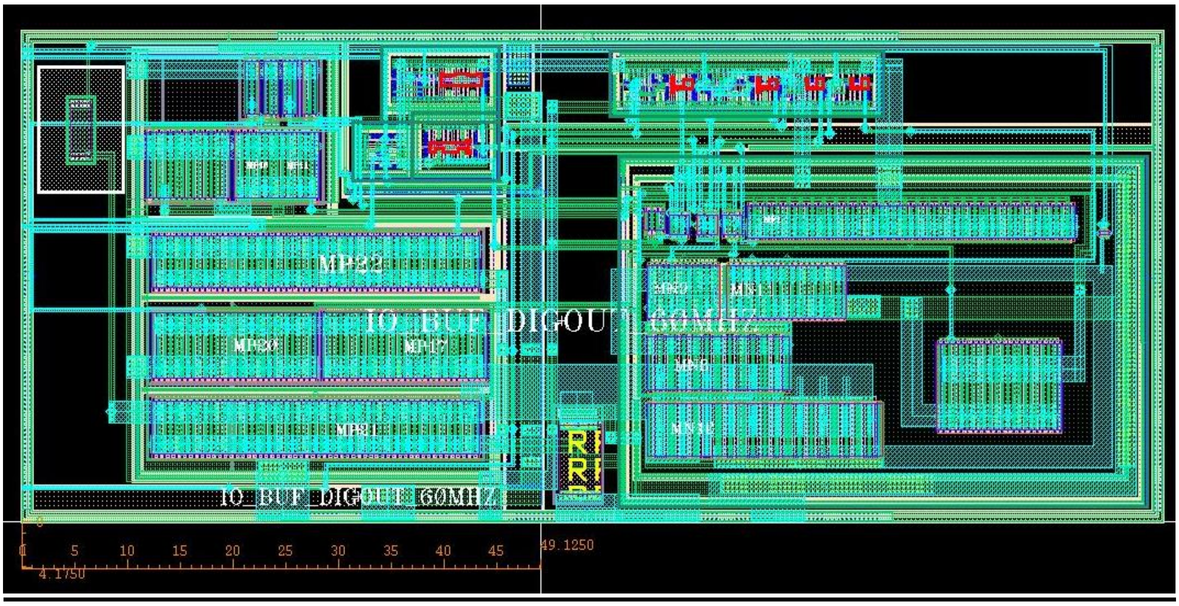

Figure 4. The layout of the proposed digital I/O pad buffer

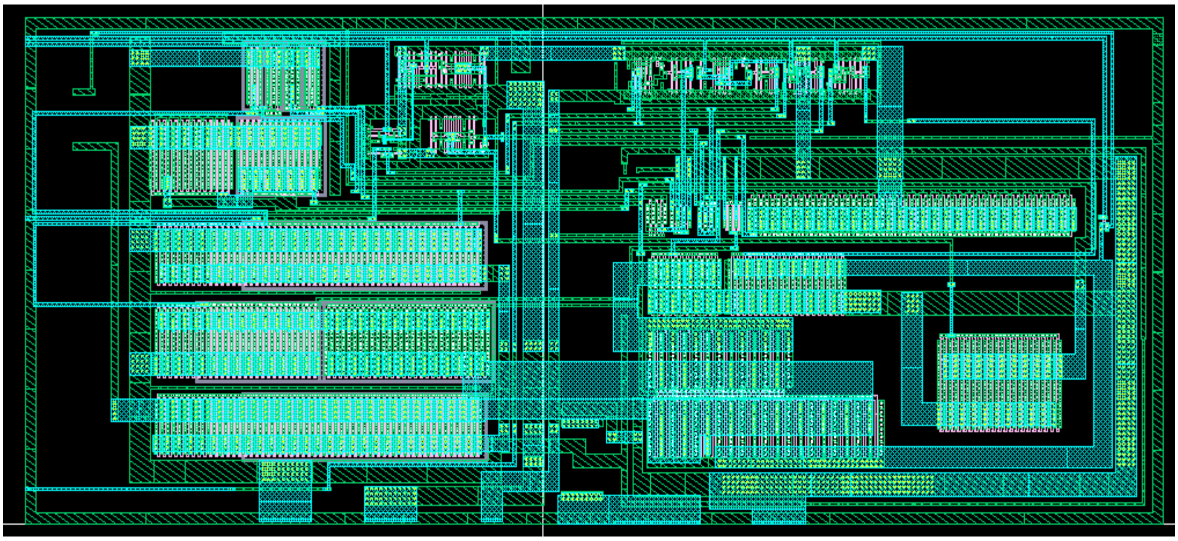

Figure 5. The extracted of the proposed digital I/O pad buffer

3.2. Post-Layout Characterization using ACS

Post-layout simulation is very useful to modify the designed digital I/O pad buffer and become closer to the measurement specifications. The proposed digital I/O buffer has been post-layout simulated using Cadence Virtuoso with drawing layout and checking DRC and LVS. The corner processes analysis is reported to demonstrate the mismatch and global process variations on the transient response of the proposed digital I/O pad buffer.

We plot the weak, strong, and typical output curves for each application case, line parameters, and the input curve. The corners are defined as described in the table 1 below:

Table 1. Defined the corners of the device

Corner	NMOS	PMOS	RESISTOR	Routing Resistor	Supplies	TEMP (deg)
"Typic"	typic	typic	typic	nom	nom	27
"Weak"	weak	weak	high	max	min	125
"Srong"	strong	strong	low	min	max	-40

a) One chip connected – High drive = ’1’ with Z0=44ohm, Td=112p

Figure 6 shows the curve voltage for Rising/ Falling edge of the proposed digital I/O pad buffer. With one chip connected – High drive = ’1’ with Z0=44ohm, Td=112p.

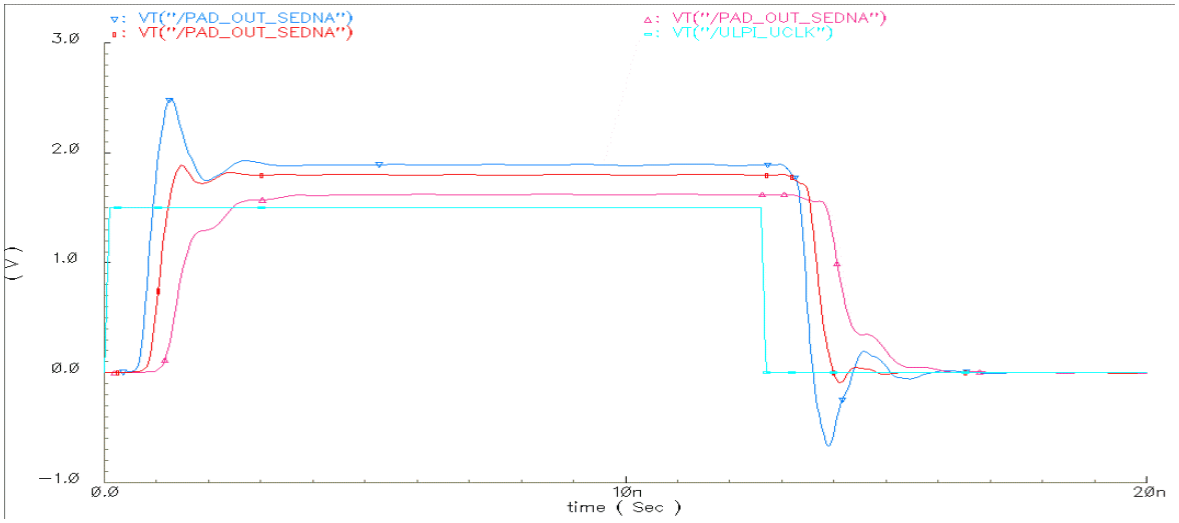

Figure 6. Curve for Rising/ Falling edge

Table 2 shows the AC characteristics of the proposed digital I/O pad buffer for Rising/ Falling edge. The delay times are simultated from the input signal (VIO) of 0.9 voltage level to the output signal (PAD) of 1.8 voltage level. As shown in Table 1, the simulated rising delay time Trise-rising are 0.42 ns with 3 pF load. The falling delay time Tfalle-falling are 0.93 ns with 3pF load. The output rising time Trisie and falling time Tfalle are defined from output rise time on test point 10%-90% and from output fall time on test point 10%-90%, respectively. As shown in Table 1, the simulated delay rising (Delay_r) are 0.93 ns with 3 pF loads. The delay falling (Delay_f) are 0.95 ns with 3 pF loads. The duty cycle D cycle is defined the pulse duration from test point 10%-90% at rise edge of the output signal (PAD) to test point 10%-90% at fall edge divided by the period of the output signal (PAD). As shown in Table 1, the simulated Dcycle are 50.9% under the load 3 pF.

Table 2. AC characteristics simulated of the digital I/O pad buffer for Rising/ Falling edge

Parameter	Description	Min	Nom	Max	Units
Freq	Input Frequency			40	Hhz
Trise	Output Rise Time on Test Point 10%-90%	0.28	0.42	1.58	ns
Tfall	Output Fall Time onTest Point 10%-90%	0.24	0.38	1.54	ns
Delay_r	Internal rise delay between IN_LOWV and Test Point – Td	0.73	0.93	1.27	ns
Delay_f	Internal fall delay between DATA_IN_LOWV and Test Point	0.73	0.95	1.33	ns
Overshoot	Maximum Overshoot on PAD and Test Point		13	326	mV
Undershoot	Maximum Undershoot on PAD and Test Point		23	421	mV
Duty Cycle	Duty cycle on test point	49.9	50.4	50.9	%

b) One chip connected – High drive =' 0' with Z0=80ohm, Td=112p.

Figure 7 shows the curve voltage for Rising/ Falling edge of the proposed digital I/O pad buffer. With one chip connected – High drive =' 0' with Z0=80ohm, Td=112p.

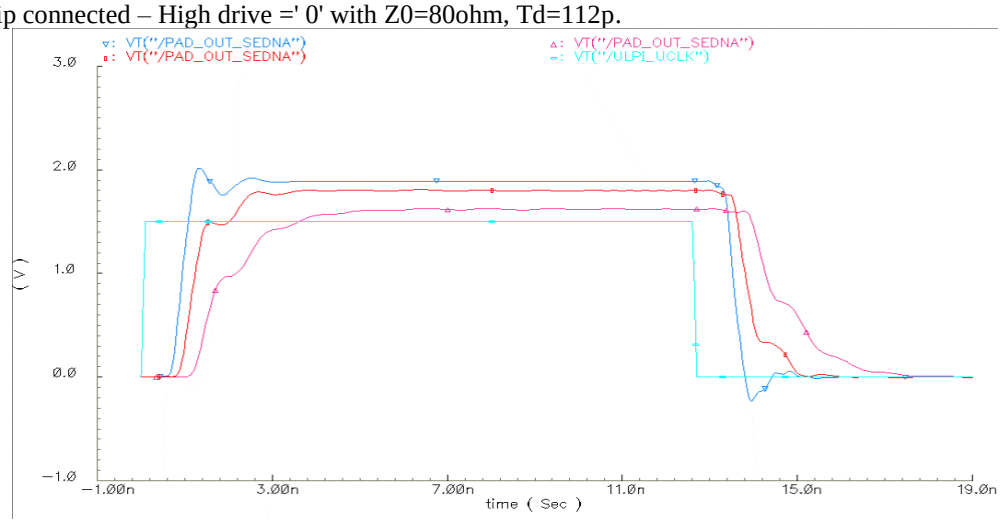

Figure 7. Curve for Rising/ Falling edge

Table 3 shows the AC characteristics of the proposed digital I/O pad buffer for Rising/ Falling edge. The delay times are simultated from the input signal (VIO) of 0.9 voltage level to the output signal (PAD) of 1.8 voltage level. As shown in Table 1, the simulated rising delay time Trise-rising are 1.57 ns with 3 pF load. The falling delay time Tfalle-falling are 0.65 ns with 3pF load. The output rising time Trisie and falling time Tfalle are defined from output rise time on test point 10%-90% and from output fall time on test point 10%-90%, respectively. As shown in Table 1, the simulated delay rising (Delay_r) are 1.09 ns with 3 pF loads. The delay falling (Delay_f) are 1.12 ns with 3 pF loads. The duty cycle D cycle is defined the pulse duration from test point 10%-90% at rise edge of the output signal (PAD) to test point 10%-90% at fall edge divided by the period of the output signal (PAD). As shown in Table 1, the simulated Dcycle are 51.2% under the load 3 pF.

Table 3. AC characteristics simulated of the digital I/O pad buffer for Rising/ Falling edge

Parameter	Description	Min	Nom	Max	Units
Freq	Input Frequency			40	Hhz
Trise	Output Rise Time on Test Point 10%-90%	0.42	1.57	2.17	ns
Tfall	Output Fall Time onTest Point 10%-90%	0.39	0.65	2.09	ns
Delay_r	Internal rise delay between IN_LOWV and Test Point	0.81	1.09	1.56	ns
Delay_f	Internal fall delay between DATA_IN_LOWV and Test Point	0.80	1.12	1.69	ns
Overshoot	Maximum Overshoot on PAD and Test Point		14	308	mV
Undershoot	Maximum Undershoot on PAD and Test Point		24	488	mV
Duty Cycle	Duty cycle on test point	49.9	50.5	51.2	%

3.3. Characterization of Current Consumptions (Reset Mode and Active mode)

The Characterizations of Current Consumptions (Reset Mode and Active mode) are shown in Tables 4 and 5.

a) Reset Mode

Table 4 shows that the current consumption in reset mode is less than 90 nA without a clock input.

Table 4. Characterization of Current Consumptions for Rest Mode

Parameter	Conditions	Nom	Max	Unit
V_{DD}_CORE_LOWV	Without Clock input	0.3	30.0	nA
V_{DD}_IO_LOWV = V_{IO}	Without Clock input	0.3	30.0	nA
V_{DD}_IO_LOWV = V_{IO}	Without Clock input	2.9	90.0	nA

b) Active Mode (High drive =' 0')

It is clear from Table 5 that the current consumptions for the active mode are less than 756 nA with clock running @40Mhz.

Table 5. Characterization of Current Consumptions for Active Mode

Parameter	Conditions	Nom	Max	Unit
V_{DD}_CORE_LOWV	With Clock running @40Mhz	64.5	79.1	nA
V_{DD}_IO_LOWV = V_{IO}	With Clock running @40Mhz	0.01	0.87	nA
V_{DD}_IO_LOWV = V_{IO}	With Clock running @40Mhz	609.7	756.0	nA

Table 6 tabulates the comparison with several prior works. The proposed design of digital bidirectional input/output (I/O) pad buffer for mixed voltage uses the least number of devices and possesses.

Table 6. Performance Comparison of input/output (I/O) pad buffer

Parameter	[9]	[10]	[11]	This work
Year	2016	2018	2019	2021
Process	130 nm	180n	180 nm	180 nm
VDD (V)	1.2	1.8	1.8	1.8
Delay falling (ns)	>100	31.7	4.81	0.93
Delay rising(ns)	>200	1.78	5.19	0.95
Duty Cycle(%)	-	-	48.3	51.2
Freq (Mhz)	-	-	-	40
Area (µm2)	-	108.8	-	5

4. CONCLUSION

In this paper, a novel design of digital bidirectional input/output (I/O) pad buffer for mixed voltage is proposed and evaluated. The proposed I/O buffer provides lower latency and a smaller layout area than conventional I/O buffers. The conventional and proposed mixed-voltage I/O buffers are designed in a 180-nm CMOS process, whose evaluation results indicate that the proposed I/O buffer achieves up to 50% reduction on propagation delay. They also indicate that the proposed I/O buffer achieves up to 40% reduction on silicon area as compared to conventional mixed-voltage I/O buffers. Several applications are implemented using the designed circuit and post layout simulation show promising results. The output rising time and falling time are 0.42 ns and 0.93 ns with 3pF load respectively. The final chip area is only 5 um^2. The presented design procedure is suitable for use in portable applications like the Internet of Things (IoT).

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