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# A Novel Design and Implementation of FBMC Transceiver for Low Power Applications

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**ABSTRACT**

The complex structure of the Filter Bank Multicarrier (FBMC) communication system is the main drawback affecting the performance of the system and causes a high-power consumption. The complexity arises from using a polyphase filter bank, which consists of fast Fourier Transform/ Inverse Fast Fourier Transform (FFT/IFFT) processors and a filter bank of Finite Impulse Response (FIR) filters. This paper presents the analysis and the implementation of a new design model for FBMC transceiver in which the polyphase filter is removed completely in both transmitter and receiver and uses instead of it, a multi-level cascaded structure of FIR subfilters. The coefficients of each subfilter selected using an optimization algorithm to minimize the amplitude of sidelobes compared to the amplitude of the main lobe in the frequency response of the subfilter. The proposed design reduces the number of multiplications compared to the conventional design by 65%. The field-programmable gate array (FPGA) implementation results indicate that the proposed architecture saves 24% of resources of the FPGA board, works faster, and saves 27% of power consumption compared to conventional FBMC transceiver.



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## 1. INTRODUCTION

FBMC is a digital multicarrier modulation technique; it provides many advantages such as reduction of inter symbolic interference (ISI) and intercarrier interference (ICI) that may introduce when using channels with varying gain in their frequency band [1-3]. Another most critical advantage of FBMC is its higher spectral efficiency when compared with the Orthogonal Frequency Division Multiplexing (OFDM) technique [4]. Conventional FBMC transceiver, which depends on polyphase filters shown in Figure 1, consists of an offset quadrature amplitude modulation (OQAM) modulator, followed by a synthesis filter bank (SFB) in the transmitter. In the receiver, it has an analysis filter bank (AFB) and an OQAM demodulator [5].

SFB implemented using the IFFT processor followed by the polyphase network (PPN) and AFB implemented by PPN, followed by the FFT processor. PPN is a group of Finite Impulse Response (FIR) filters which, when united, form the impulse response of a prototype filter [6]. From Figure 1, PPN in the SFB in the transmitter consists of N number of FIR filters. Each FIR filter output followed by (N/2) up-samplers and delay units. All filters output summed to form the transmitter signal while PPN in AFB in the receiver consists of delay units, down-samplers (N/2), N FIR filters, and FFT processor. For FBMC transceiver, implementation of FFT, IFFT, and FIR filters requires a large number of multipliers and adders,

which increases the complexity of the system, causes a high-power consumption, and reduces the overall speed of transmission [7].

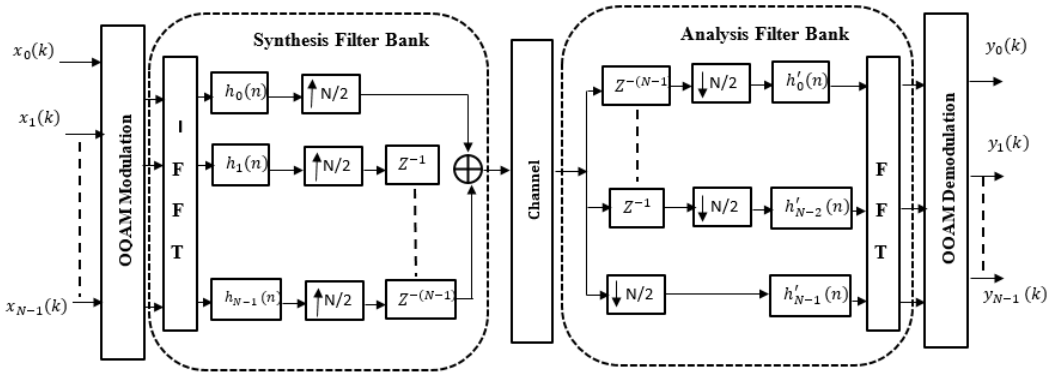


Figure 1. Conventional FBMC Transceiver

The complexity in the hardware model can be measured by the total number of multiplications, additions in the design. In the conventional structure, as shown in Figure 1, the number of subscribers (N) is the length of FFT/IFFT, and the overlapping factor is (K) [8]. The total complexity requirements of the conventional method are:

$$Number\ of\ Multiplications = 4(N(log_2 N - 3) + 4 + 2NK) \quad (1)$$

Many methods proposed to reduce the complexity of the FBMC system. In [9], the two real input symbols combined to form one complex input symbols which lead to a reduction in the size of IFFT processors. For separation, the output of the IFFT into real and imaginary parts, multiplication by ½, and extra additions are required. The complexity of this method (Reduced Method I) can be derived as:

$$Number\ of\ Multiplications = 2\ [(log_2 N - 3) + 4 + 4NK] \quad (2)$$

Another method to reduce the complexity of conventional design presented in [10]; the idea of this work utilizes the symmetry between odd and even indices of the IFFT. From the computational complexity, it has a lower cost only to calculate the even indices and design a pruned IFFT structure which cancels the unneeded calculations of the IFFT butterflies, and then data will be extended by calculating samples of the odd indices from the results of the even indices. The complexity of this method (Reduced Method II) can be derived as:

$$Number\ of\ Multiplications = 4\ [\tfrac{N}{2}(log_2 \tfrac{N}{2} - 3) + 4 + 2NK] \quad (3)$$

Another suggested method to reduce the complexity of conventional FBMC transceiver done by using a feedback loop with (N) to compute FFT for $(2^N)$ points, and implementing FIR filters by using distributed arithmetic technique [11]. Another method reduces the FBMC complexity used the variant of the sliding DFT or hoping DFT presented in [12]. Another idea replaces the two full-size IFFTs by two half-size IFFTs depending on the real-valued data processing is presented in [13]. A new pipelined design of the FBMC transmitter which reduces the memory resources and computation compared to the conventional one presented in [14].

This paper proposed a new design for FBMC transceiver, which removes and replaces the SFB in the transmitter and the AFB in the receiver with a multi-level cascaded structure of FIR sub-filters. The cascaded sub-filters in the transmitter called Transmitter Filters Network (TFN), while the cascaded sub-filters in the receiver called Receiver Filters Network (RFN). The coefficients of each sub-filter in TFN and RFN are chosen to reduce the amplitude of side-loops in the frequency response of each filter. The conventional design of FBMC transceiver and the proposed design are implemented using the FPGA board, and the simulation results indicate a reduction in power consumption as a result of reducing the number of multipliers in the proposed design.

This paper organized as follows: Section 2 introduces the structure and mathematical analysis of the cascaded filter structure. Section 3 the simulation and comparisons between the conventional and proposed design. Section 4 FPGA implementation of the proposed design. Section 5 Implementation results and comparison between different methods used to reduce complexity. And finally, the conclusion is presented in section 6.

## 2. PROPOSED FBMC TRANSCEIVER

The idea of replacing the first order prototype filter of the FFT with a higher-order prototype filter presented in [15], but it did not employ or tested for the FBMC transmission system. The proposed design removes the IFFT/FFT processors in both transmitter and receiver, and replaces the PPN in the transmitter by a transmitter filters network (TFN), and replacing the PPN in the receiver with receiver filters network (RFN). Both TFN and RFN are a network of cascaded FIR sub-filters. The block diagram of the FBMC transceiver for the eight subscribers or sub-channels is shown in Figure 2.

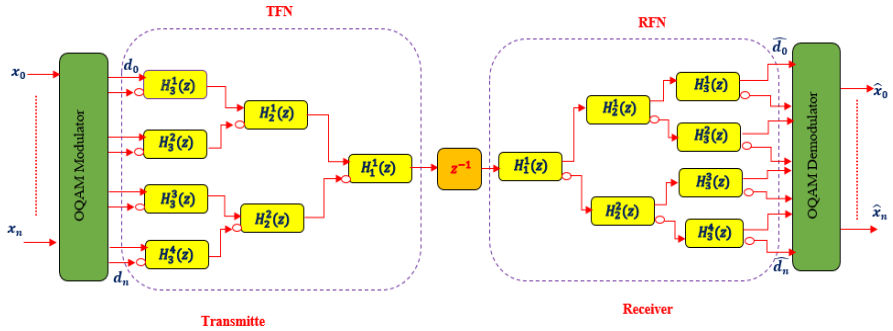


Figure 2. Proposed FBMC System

The difference between the conventional and proposed transceiver is removing the SFB and AFB and replace both of them by the TFN and RFN, respectively. The proposed transceiver consists of a transmitter, a delay unit as a channel and a receiver. The transmitter is an Orthogonal Quadrature Amplitude Modulation (OQAM) modulator unit, and TFN, while the receiver is RFN, and an OQAM demodulator unit.

The input to OQAM modulator module is a stream of binary data; (1,0,1,0,…..) and the output is purely real or imaginary converted from serial to parallel as shown in the following equation

$$d_n = \begin{cases} 1, j, 1, j, \dots\dots \ n\ even \\ j, 1, j, 1, \dots\dots n\ odd \end{cases} \quad (4)$$

Then the modulated sequences are converted from serial to parallel and distributed as input to the TFN. The output signal sequences of TFN are then delayed before inserting into the receiver, which has a symmetrical reversed structure as that of the transmitter. The received sequence passes through RFN, and OQAM demodulator. The demodulator receives the estimated sequence $(\widehat{d_0}, \widehat{d_1}, \dots\dots \widehat{d_n})$ and finally produces the output signals $\hat{x}_0, \dots, \hat{x}_n$. Each subfilter in the TFN and RFN has the following properties:

1- Odd length symmetrical impulse response half-band FIR filter.

2- Noncausal; have values for n<0. The FIR filter described in Z-domain and time domain as:

$$H_k^m(z) = \sum_{n=-\infty}^{\infty} h_k^m \, Z^{-n} \quad (5)$$

$$h_k^m(n) = h_k^m(-n) \quad (6)$$

Where $h_k^m(n)$ is the impulse response of a subfilter, k: number of levels, m: number of filters in a level.

The number of levels $(k)$ can be calculated using the number of subcarriers (N) as

$$k = \log_2(N) \quad (7)$$

And the number of sub-filters is N-1.

3- Complementary filter which means it produces two outputs the normal output and the complementary output. Figure 3 shows the block diagram of a sub-filter in the proposed structure.

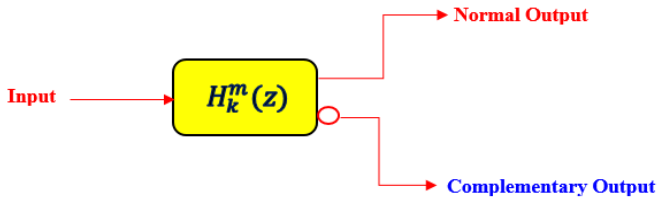


Figure 3. Block diagram of FIR filter

With the non-causal filter, we can define

$$H_k^m(z) + H_{kc}^m(z) = 2 \quad (8)$$

Where $H_{kc}^m(z)$ : is the complementary FIR filter of $H_k^m(z)$, and it represents a high pass filter.

For a number of eight sub-channels, RFN is shown in Figure 4, each subfilter receives one input and produces two outputs the normal, and complementary output. Figure 5 shows TFN for the eight subchannels. The structure is the same as RFN with the reverse directions of inputs and outputs. Each subfilter in the network is a single input multiple outputs.

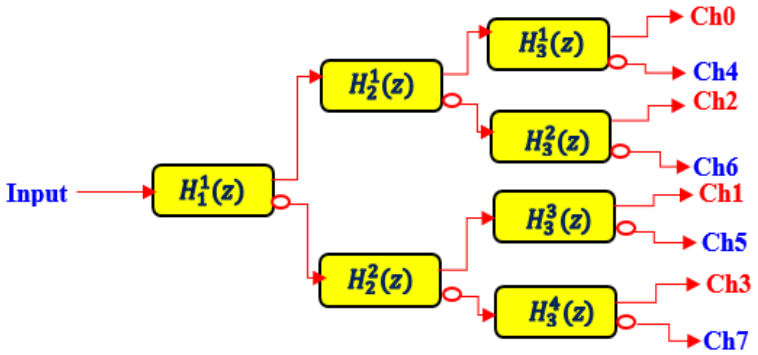


Figure 4. Block diagram of RFN for eight subchannels

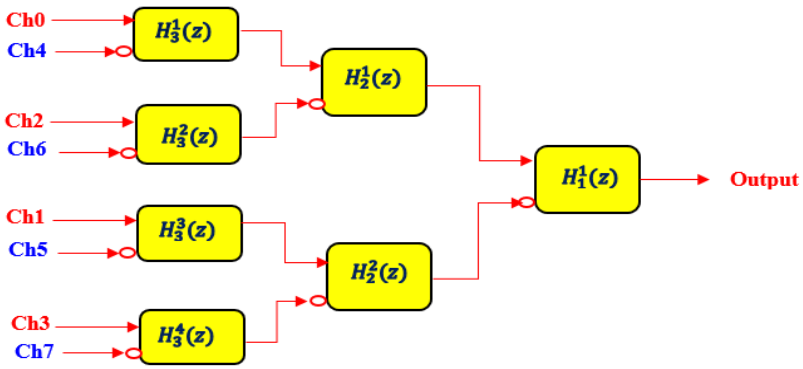


Figure 5. Block diagram of TFN for eight subchannels

The equation of each sub-filter in TFN in the transmitter considered as the same in the RFN in the receiver with reversing the directions of input and output signals. RFN composed of seven low pass FIR filters distributed into three levels. The output channels are orders using a bit reverse order method as in FFT. As an example to calculate the transfer function of the output channels, the first channel transfer function ($Ch_o(z)$) can be calculated as follows:

$$Ch_0(z) = H_1(z)H_2(z)H_3(z), \quad (9)$$

Where,$H_1(z) = H_1^1(z)$, $H_2(z) = H_2^1(z) = H_2^2(z)$, $H_3(z) = H_3^1(z) = H_3^2(z) = H_3^3(z) = H_3^4(z)$

While the transfer function of the fifth channel ($Ch_4(z)$) is

$$Ch_4(z) = H_1(z)H_2(z)H_{3c}(z) \quad (10)$$

Where, $H_{3c}(z)$ is the complementary output of $H_3(z)$.

And the transfer function of the last channel ($Ch_7(z)$) is

$$Ch_7(z) = H_{1c}(z)H_{2c}(z)H_{3c}(z)$$

(11)

Where, $H_{1c}(z), H_{2c}(z)$ are the complementary output of $H_1(z)$, and $H_2(z)$ respectively.

One of the main demands in filter bank design is Perfect Reconstruction (PR) which means that the signal doesn't get corrupted by the filter bank. Considering the proposed cascaded network is one type of uniform filter banks, the frequency responses of the channels are the shifted versions of that of the first channel.

In FIR filters design of the proposed network, to achieve the PR, it can be considered as optimization equation in which the amplitude of side lopes which results from inter-symbol interference (ISI) and inter-channel interference (ICI) has to be minimized according to the predefined ripples in the passband ($r_p$) [16]. The process of determining the coefficients of sub-filters of the proposed network is generated as follows:

1- Assuming the values of $r_p, r_s$ the ripples in passband and stopband respectively.

$$1 - r_p < \left|H_0(e^{j\omega})\right| < 1 + r_p \qquad |\omega| \le \omega_p \quad (12)$$

$$\left|H_0(e^{j\omega})\right| < r_s \qquad \omega_s \le |\omega| \le \pi \quad (13)$$

Where: $\omega_p$: passband frequency, $\omega_s$: stopband frequency, $|H_0(e^{j\omega})|$ : Amplitude of frequency response of channel 0.

2- Solving the following optimization equation

$$\text{Min}(\epsilon_{max}) = \frac{1}{f_{ch0}(0)} \left\{ \sum_{n\neq 0} |f_0(n)| + \sum_{n} \sum_{n_0=1}^{N-1} \left|f_{chn(n)}\right| \right\} \quad (14)$$

where

$$f_{chn}(n) = real\left(d_{chn}^{*}.h\left(n.\frac{N}{2}\right)\right) \quad (15)$$

$h(n)$ : The impulse response of ( $h_1(n) * h_{chn}(n)$)

$\epsilon_{max}$: the maximum amplitude of the side lobes
$N$ : the channel number.

The results of solving Eqn. (15) is shown in Table 1.

Table 1. Sub-filters coefficients of RFN

| n | $h_1(n)$ | $h_2(n)$ | $h_3(n)$ |
|---|---|---|---|
| 0 | 1 | 1 | 1 |
| ±1 | -0.0172 | 1.6352 | -0.7278 |
| ±2 | -0.0573 | 1 | 0.1780 |
| ±3 | 0.06 | | |
| ±4 | 0.293 | | |
| ±5 | 0.2619 | | |
| ±6 | 0.1067 | | |

The complexity of proposed FBMC transceiver can be expressed as

$$Number\ of\ Multiplications = 4 \times 2 \times 2 \sum_{i=1}^{K-1} 2^{(i-1)} L_i \quad (16)$$

Where $L_i$ is the filter length of the sub-filter. Eqn. (16) can be clarified as follow:

Multiplication by four because the complex multiplier contains four real multipliers. Multiplication by the first two because the number of multiplications of TFN is equal to a number of multiplications of RFN. Multiplication by second 2, because of the number of multiplications for normal output equal to the number of multiplications of complementary output.

## 3. SIMULATION RESULTS

The performance of the proposed design investigated through a comparison between the conventional FBMC transceiver with overlapping factor (K=4) and the proposed transceiver. Figure 6 shows a comparison between the impulse response of the prototype filter in conventional FMBC and the proposed transceiver. It is clear that the proposed filter network has a narrow transition bandwidth than the conventional one.

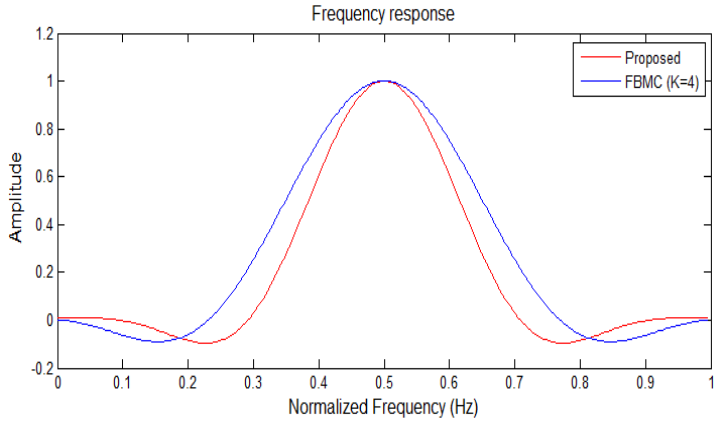


Figure 6. The frequency response of the proposed structure and conventional FBMC

The system simulated with eight sub-channels. The number of complex OQAM symbols is set to 10000 symbols randomly generated. The passband frequency is 150 kHz with passband ripples ($r_p = 0.01\ dB$), and the stopband frequency is 300KHz with stopband ripples ($r_s = 45\ dB$). Figure 7 shows the frequency response of eight sub-channels.

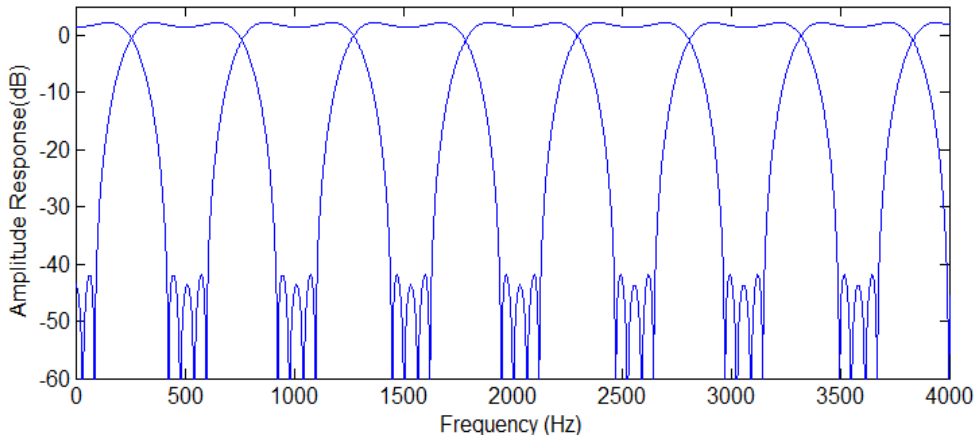


Figure 7. Frequency response eight subchannels of the proposed structure

The constellation diagram of the output signal $\hat{d}_n$ for the proposed FBMC transceiver is illustrated in Figure 8, it is clear that the output data are identical to input data without any mismatch. A comparison between the proposed and conventional systems to investigate the Bit Error Rate (BER) versus a range of bit to noise ratio (EbN0dB) is made and illustrated in Fig.9. As shown in Figure 9 the BERs are identical and no degradation in the performance of the proposed system compared to the conventional one.

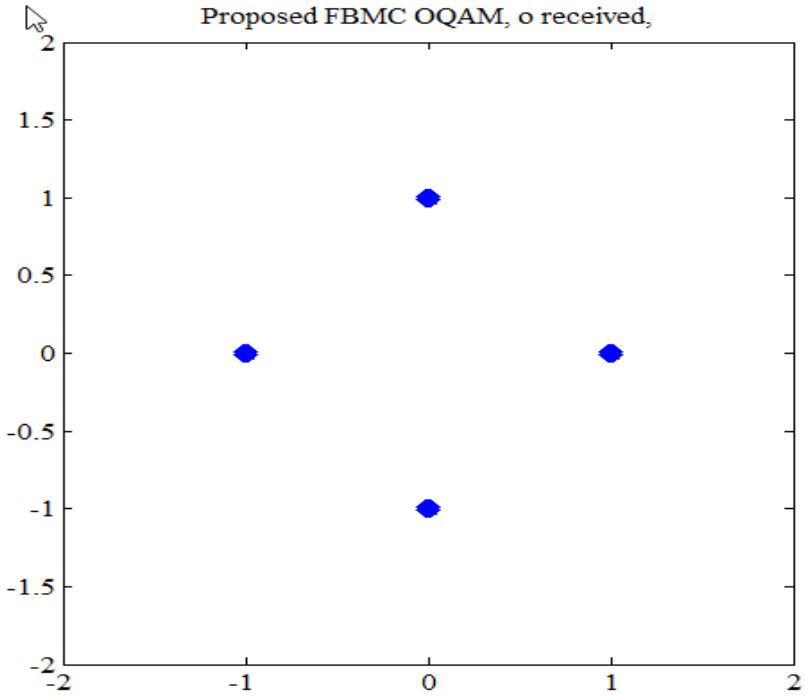


Figure 8. Constellation diagram of the output signal

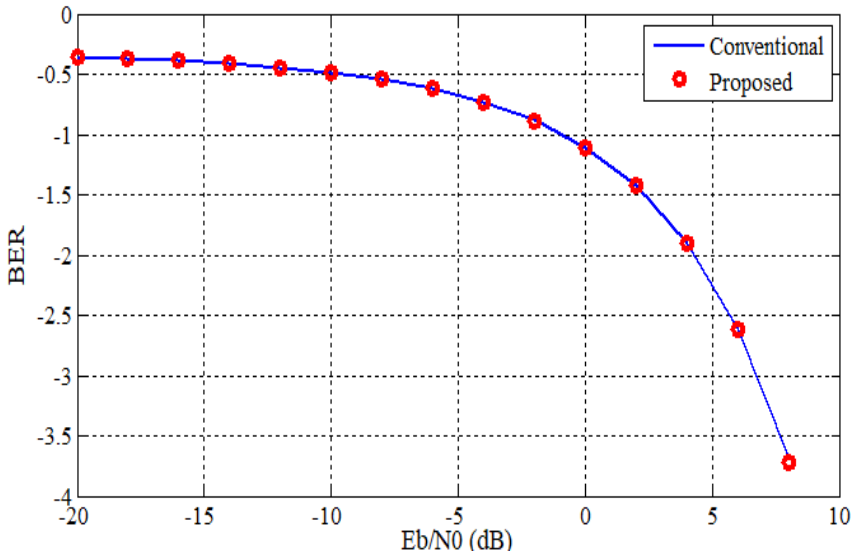


Figure 9. BER Vs. EB/N0 (dB) for proposed and conventional systems

The main advantage of the proposed transceiver is the big reduction in the number of multipliers compared to conventional architecture, especially in case of a large number of subscribers. Table 2 shows a comparison between the proposed design and the different methods used to reduce the complexity of the conventional structure.

Table 2. Complexity comparison between different methods to implement FBMC

| Method | $h_1(n)$ | $k=4$ | | | |
|---|---|---|---|---|---|
| | | *N=64* | N=128 | N=256 | N=512 |
| Standard Polyphase (Conventional) [8] | $4(N(\log_2 N-3)+4+2Nk)$ | 2832 | 6160 | 13328 | 28688 |
| Reduced Method I [9] | $2(N(\log_2 N-3)+4+4Nk)$ | 1412 | 3076 | 6660 | 14340 |
| Reduced Method II [10] | $4\,[\frac{N}{2}(\log_2 \frac{N}{2}-3)+4+2NK]$ | 1160 | 2440 | 5128 | 10760 |
| Proposed | $4\times 2\times 2\sum_{i=1}^{K-1} 2^{(i-1)}L_i$ | 975 | 1904 | 4090 | 8492 |

From table 2, the proposed method reduces around 70 % of multiplications compared to conventional structure, saves around 40 % of multiplications compared to "Reduced Method I", and saves around 20 % of multiplications compared to "Reduced Method II".

## 4. FPGA IMPLEMENTATION

Xilinx System Generator (XSG) is a library integrated inside Simulink program that allows creating, designing, simulating and generating a VHDL code for a digital hardware model realized to describe the operation of digital systems [17]. The main advantages of XSG are the simplicity to generate a VHDL code for complex hardware systems and the ease of providing synchronization between different components of the model in a graphical user interface (GUI) environment, which consider as a difficult task in complex digital systems [18-19]. Another advantage provided by XSG is hardware co-simulation in which a hardware model implemented into FPGA board can be simulated in the program environment. In this paper, the proposed, conventional, and different methods used to reduce complexity are implemented on the same FPGA board (Xilinx Vitrex-7 XC7VX550t board), and the implementation results will be examined. The parameters of FBMC transceiver used in implementation are listed in Table. 3.

Table 3. FBMC Parameters for Hardware Model

| Parameter | Value |
|---|---|
| Total Bandwidth | 5 MHz |
| *Sample rate* | 1 MHz |
| Number of subchannels (subcarriers) | 8 |
| Overlapping factor (K) | 4 |
| "Not used for proposed design" | |

The architectures are modeled using 32 fixed-point format. The speed of operation is the main feature of using the fixed-point format in arithmetic operations instead of using a floating-point format. In different applications where high accuracy is not required, the fixed-point format is used [20]. Figure 10 shows the XSG hardware model of one sub-filter in RFN.

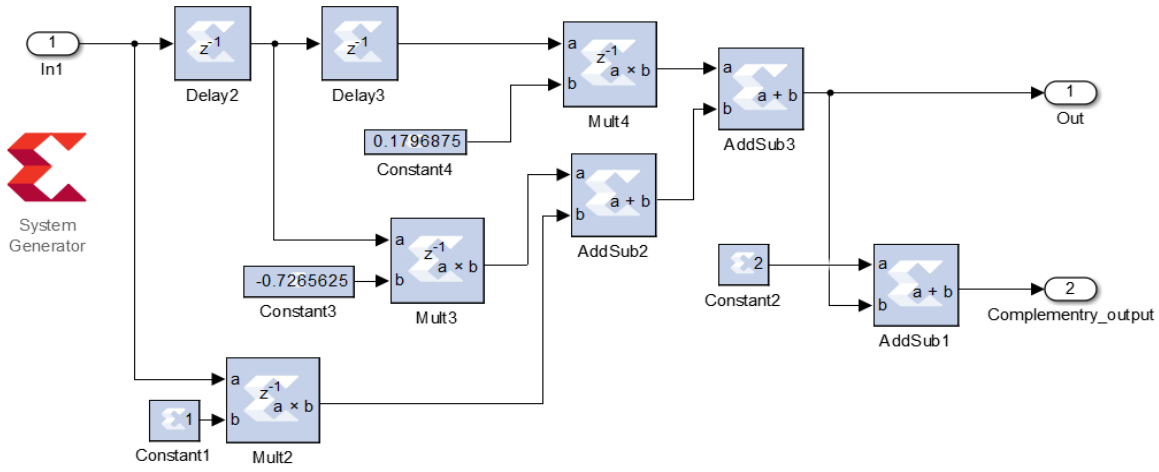


Figure 10. XSG hardware model of subfilter $h_3(n)$

## 5. IMPLEMENTATION RESULTS

### 5.1. Behavioral Simulation

In this type of simulation, the validity of the proposed hardware model will be tested by performing the same type of simulation that has been investigated by the Matlab code. Figure11 shows the magnitude square (dBW/Hz) of the first channel generated by the hardware model, as seen in Figure11; the result agrees with the theoretical simulation and the sidelobes appear at – 45 dB as expected. Figure12 shows the magnitude squared of the spectrum of the transmitted signal generated by the proposed hardware model.

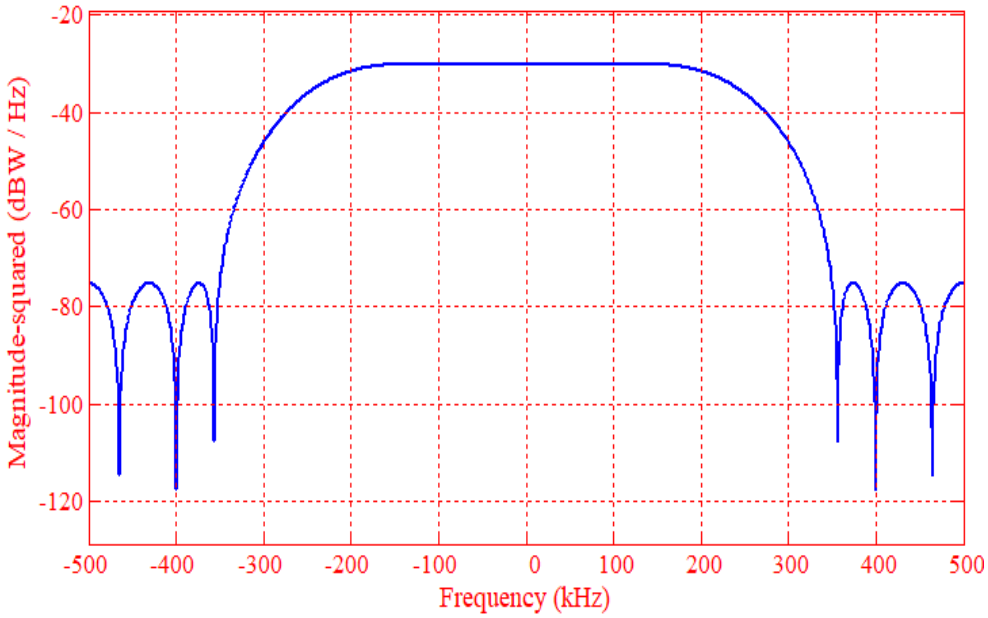


Figure 11. Magnitude squared of the first channel generated by proposed hardware model

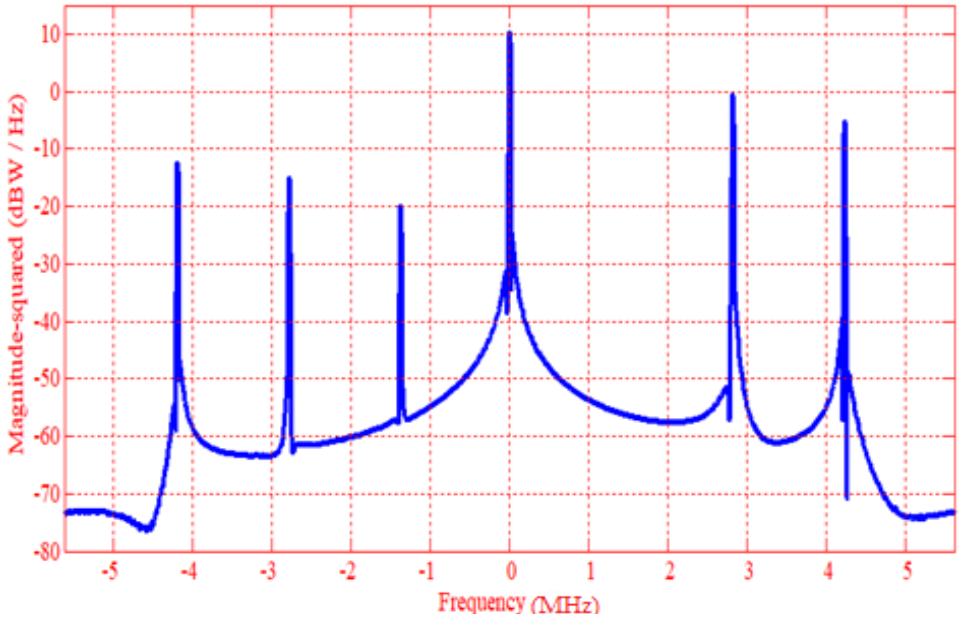


Figure 12. Magnitude squared of the spectrum of the transmitted signal

### 5.2. Implementation Results

The device utilization report, which indicates how much resources (Registers, LUT, LUT flip-flops) of the FPGA device are used to implement the hardware model of the FBMC transceiver architecture, is the main topic of this paper. A comparison between the three-hardware model is done and presented in Table 4.

Table 4. Comparison between different hardware models

| Architecture | *No. of Slice Registers* | *No. of Slice LUTs* | *No. of fully used LUT-FFs* | *Max. Frequency (MHz)* | *Power (mWatt)* |
|---|---|---|---|---|---|
| Standard Polyphase (Conventional) [8] | 846 | 1565 | 2073 | 238 | 302 |
| Reduced Method I [9] | 790 | 1388 | 1876 | 243 | 254 |
| Reduced Method II [10] | 779 | 1302 | 1790 | 247 | 242 |
| M. Saber [11] | 740 | 1230 | 1778 | 248 | 237 |
| Proposed | 646 | 1189 | 1510 | 255 | 221 |

## 6. CONCLUSION

This paper introduced a new design and implementation for FBMC transceiver by removing the polyphase network in both transmitter and receiver and replaced it by a network of cascaded FIR filters. The proposed architecture has been explained and analyzed with the required mathematical model and equations. The validity of the proposed design has been investigated and compared to the conventional and different previous methods proposed to reduce the complexity of the design. Comparison results indicate that the proposed design the proposed method reduces around 70 % of multiplications compared to conventional structure, saves around 40 % of multiplications compared to "Reduced Method I", and saves around 20 % of multiplications compared to "Reduced Method II". Reduction of the total number of multiplications in the transceiver means a reduction in the complexity and design of the system. The proposed and conventional architectures have been designed using XSG program and implement into the same FPGA board, Vertix-7 XC7VX550t. The implementation results indicate that the proposed model compared to the Conventional one, provides a 24% reduction in the number of registers, and 24% reduction in the number of LUT, works at higher power frequency and saves 27% of consumed power.

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