Indonesian Journal of Electrical Engineering and Informatics (IJEEI)
Vol. 8, No. 3, September 2020, pp. 447~456
ISSN: 2089-3272, DOI: 10.11591/ijeei.v8i3.1766

A New Topology of a Single-Phase Five-Level Inverter

L. Heru Pratomo
Department of Electrical Engineering, Soegijapranata Catholic University, Indonesia

Article Info

Article history:
Received Oct 30, 2019
Revised Jun 11, 2020
Accepted Aug 3, 2020

Keyword:
New topology
Five-level
Inverter
Single-Phase
Four active switches

ABSTRACT

The power inverter technology with low harmonics content is used for many applications, such as in new and renewable energy sector. In the last decades, some researchers explored its inverter to minimize the harmonics content, and one of the solutions is a five-level inverter. A single-phase five-level inverter has a good performance in power conversion and improved performance. Nevertheless, the conventional five-level inverter topology always deals with many power semiconductor switches and a complex control algorithm. This paper, therefore, presents a new topology of a five-level inverter using four active switches. The new topology can work well as a single phase-five-level inverter with a novel Sinusoidal Pulse Width Modulation (SPWM) control algorithm using level-phase shifted carrier strategy. The new inverter has a simple power circuit and control strategy. The verification of this research is a simulation and prototype implementation, carried out in a laboratory. The results show that the proposed control strategy is capable of achieving five-level with a simple control strategy.

Corresponding Author:
L. Heru Pratomo,
Department of Electrical Engineering,
Soegijapranata Catholic University,
Jl. Pawiyatan Luhur IV/1 Bendan Nduwur Semarang, Jawa Tengah, Indonesia
Email: leonardus_hp@yahoo.com

1. INTRODUCTION

In the last decades, researchers explored a single-phase inverter to achieve high performance, which results in the small harmonic content on the output side, simple control, low cost, and high efficiency. Conventional inverter designs therefore utilize an H – bridge inverter. To achieve a small harmonic content on the output side (voltage or current), it must operate at high frequencies, utilizing a large passive filter. One disadvantage of a multilevel inverter is the complex and many active switches. Two other disadvantages of a multilevel inverter are the fact that the small voltage stages are typically designed by isolating voltage sources or many bulk capacitors and the inherent difficulty of algorithm control [1-3]. Due to these limitations, single-phase five-level inverters are widely studied and developed. This topology of an inverter is the same as the H-bridge inverter with the same operational function as an energy conversion from DC to AC voltage. However, it has a better Total Harmonic Distortion (THD) output performance, even though they are less efficient due to the high number of active power semiconductor devices.

The several types of a single phase five level inverters: neutral diode clamped [4-6], flying capacitor inverter/multi-cell inverter [7], and separated cascade H-bridge DC source [8]. The other type of single-phase five-level inverter is based on a combinational dual buck DC-DC converter – H bridge inverter [9, 10] or single buck DC-DC converter – H bridge inverter [11-13]. To develop a single-phase five-level inverter, many active switches are commonly needed. The researchers investigated a single-phase five-level topology: Eighty-six active switches [10, 14-17], six active switches [18, 20], six active switches and two passive switches [9, 10], five active switches and one passive switch [12, 13, 21], as well as five active switches and four passive switches [18-22]. The other topology uses four active switches [23], two passive switches, two inductors with mutual inductance and single supply DC source. It would be very difficult to implement the same inductance which has mutual inductance. The hardware setup will be more inconvenient with difficult control circuits. Many types of a single-phase five-level inverters have the same functionality in voltage and current output waveform at the same level, but the inconvenience of control and topology could be lessened. The other advantages of a new single-phase five-level inverter is low switching losses on the active component. The value of the filter size depends on frequeny switching and magnitude of the fundamental voltage. In the application of an inverter such as the grid-tie connection [24-27], a low THD is a great demand because it reduces the interference in the distribution network [28,29].

In this paper therefore a new topology of single-phase five-level inverter using four active and passive power switches is analyzed to develop a new SPWM control strategy capable of achieving a five-level output and producing higher switching frequency. This topology uses four active switches, so that it will contribute to the ease in terms of control systems, prices, shapes and sizes. A new topology of single-phase five-level inverter and a novel control strategy was validated using simulation, and at the ending step, hardware execution is carried out.

2. RESEARCH METHOD

The new topology of a single-phase five-level inverter is divided into two legs. Each leg consists of two active and passive switches. Figure 1 shows the power circuit of a new five-level inverter topology; The construction of a novel sinusoidal pulse width modulation control strategy by applying mode of operation on positive and negative cycles.

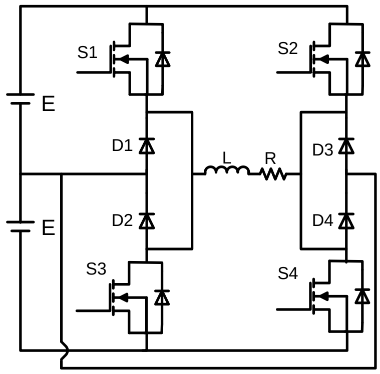

Figure 1. A new single-phase five-level inverter power circuit.

2.1 Operation mode

The principle operation of a new single-phase five-level inverter power circuit has the following Figure 2-6:

Operation Mode 1: Maximum positive output (+2E): when the active MOSFETs (S1 and S4) are conducted, the current flows from a voltage source (+2E) to the load and goes back to the voltage source. Figure 2 shows the principle of the operation mode (1) and the equation (1) is shown in this condition:

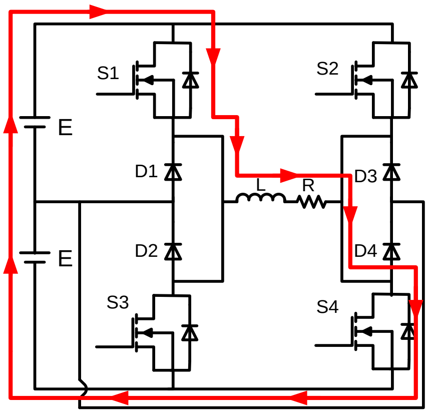

Figure 2. Operation mode 1

$$2E = v_L + V_o$$
$$L\frac{di_L}{dt} = 2E - V_o$$
$$L\Delta i_L = (2E - V_o)t_{on} \tag{1}$$

Operation Mode 2: Maximum positive output (+E): when the diode (D1) and active MOSFET (S4) are conducted, the current flows from a voltage source (E) to the load and goes back to the voltage source (E). Figure 3 shows the principle of the operation mode (2) and the equation (2) is shown in this condition:

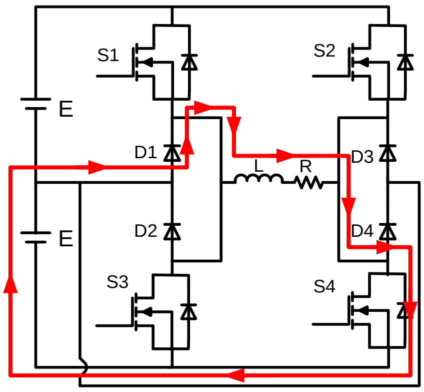

Figure 3. Operation mode 2

$$E = v_L + V_o$$

$$L\Delta i_L = (E - V_o)\Delta t$$

$$L\Delta i_L = (E - V_o)t_{on} \tag{2}$$

Operation Mode 3: The current flows in a freewheeling condition of the load for a positive value; the active MOSFETs: S4 and S3 are conducted. Figure 4 (a) shows the principle of the freewheeling condition for a positive value, and the voltage on load is 0E. While the combination of the active MOSFETs (S1 and S2) results in a freewheeling condition for a negative value, and the voltage on load is 0E. Figure 4 (b) shows the principle of the operation mode (3). This condition is shown in the equation (3):

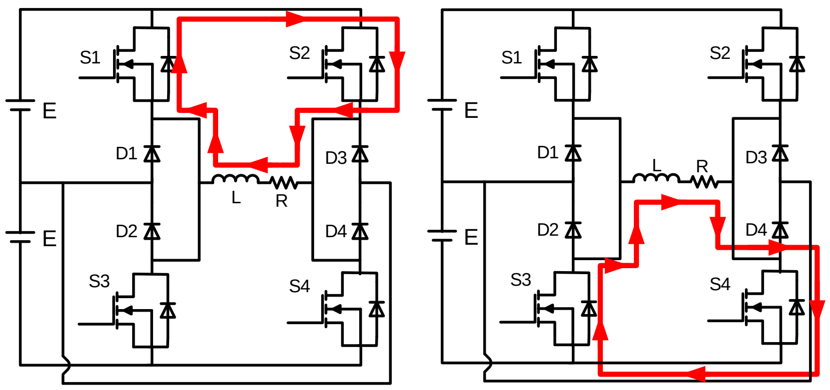

Figure 4. Operation mode 3. (a). Half of a positive cycle, (b) Half of a negative cycle

$$v_L = V_o - v_d$$

$$L\Delta i_L = V_o\Delta t$$

$$L\Delta i_L = V_o t_{off} \tag{3}$$

Operation mode 4: Maximum negative output (-E): when the diode (D3) and active MOSFET (S3) are conducted, the current flows from a voltage source (E) to the load and goes back to the voltage source. Figure 5 shows the principle of the operation mode (4) and the equation (2) is shown in this condition:

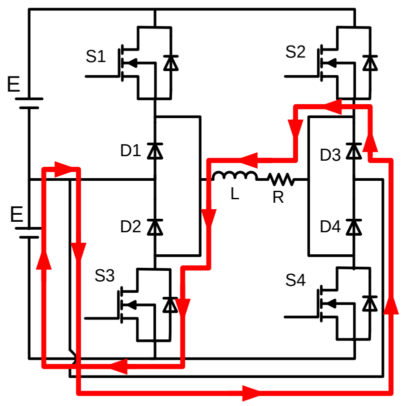

Figure 5. Operation mode 4

$$-E = v_L + V_o$$

$$L\Delta i_L = (V_o - E)\Delta t$$

$$L\Delta i_L = (V_o - E)t_{on} \tag{4}$$

Operation mode 5: Maximum negative output (-2E); when the active MOSFETs (S2 and S3) is conducted, the current flows from a voltage source (2E) to the load and goes back to the voltage source. Figure 6 shows the principle of the operation mode (5) and the equation (5) is shown in this condition:

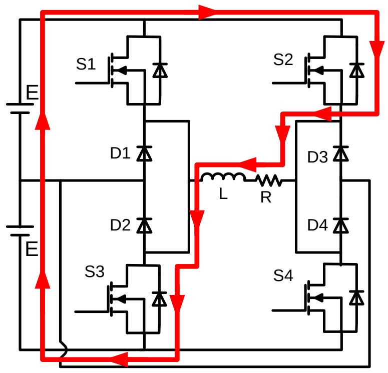

Figure 6. Operation mode 5

$$-(2E) = v_L + V_o$$
$$L\Delta i_L = (V_o - 2E)\Delta t$$
$$L\Delta i_L = (V_o - 2E)t_{on} \tag{5}$$

Finally, the matrix function is represented in the equation (6)

$$V_o = \begin{bmatrix} m_1 \\ m2 \end{bmatrix} 2E$$

$$V_o = M\,2E \tag{6}$$

which : M : The index modulation.

m_1 : $(0 \le m_1 \le \frac{1}{2})$.

m_2 : $(\frac{1}{2} \le m_2 \le 1)$.

The high frequency signal fluctuates positively and negatively. The switching of the inverter period is expressed as:

$$T = \frac{1}{f} = t_{on} + t_{off} \tag{7}$$

The output ripple current in single-phase five-level equation for the first level (0E) to the second level (E) and the second level (E) to third level (2E) are as follows:

$$\Delta i = \frac{(E - V_o)\, V_o}{E\, L\, f}$$

$$\Delta i = \frac{E\,(1 - M)}{L\, f} \tag{8}$$

Equation of the output ripple current (8) is valid at the interval time: $0 \le m_1 \le \frac{1}{2}$ and $\frac{1}{2} \le m_2 \le 1$.

which: Δi : output current ripple.

f : switching frequency.

L : inductance of inductor.

2.2 A New SPWM Control Strategy

The operation modes (1 - 5) are described above; the active switches (S1 – S4) and passive power semiconductor switches (D1 – D4) operate at high frequency. The switching table for five-level operation modes are represented in Table 1.

Table 1. Five-level inverter output

Leg 1				Leg 2				
S1	**D1**	**S3**	**D2**	**S2**	**D3**	**S4**	**D4**	**Vo**
On	**OFF**	**Off**	**Off**	**Off**	**Off**	On	**Off**	**2E**
Off	On	**Off**	**Off**	**Off**	**Off**	On	**Off**	**E**
On	**Off**	**Off**	**Off**	On	**Off**	**Off**	**Off**	**0**
Off	**Off**	On	**Off**	**Off**	**Off**	On	**Off**	**0**
Off	**Off**	On	**Off**	**Off**	On	**Off**	**Off**	**-E**
Off	**Off**	On	**Off**	On	**Off**	**Off**	**Off**	**-2E**

The generation of the SPWM gating signals for the new five-level inverter topology was carried out by applying the parameters in Table 1 to design for the proposed novel SPWM using two leg control strategies. The proposed novel SPWM control circuit for the new proposed five-level inverter is shown in Figure 7. A novel SPWM control for gating signals: S1, S2, S3, and S4 for developing a five-level inverter output waveform is illustrated in Figure 8.

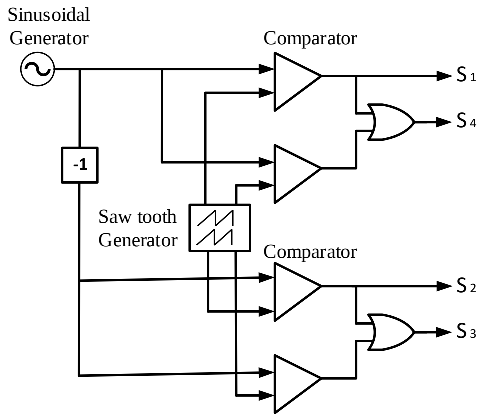

Figure 7. The proposed a novel SPWM gating sinyal control

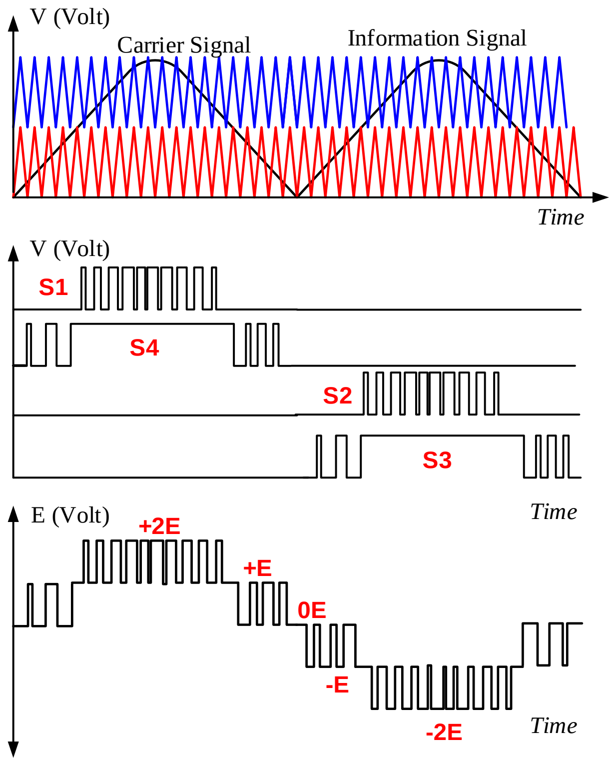

Figure 8. The constructing of five-level inverter output

3. RESULTS AND DISCUSSION

The validation of the results was conducted in the laboratory through simulation and hardware tests of the proposed new five-level inverter design using a novel SPWM control strategy. The proposed a single-phase five-level inverter is simulated with the use of Power Simulator software. The parameters used in the simulation process and laboratory test are represented in Table 2.

Table 2. Parameters for simulation and laboratoty test

Parameters	Value
Voltage source	200 Volt
Inductance filter	2 Mh
Load resistance	100 Ohm
Frequency Switching	10 KHz
Output frequency	50 Hz

The SPWM signals on active switches S3 and S4, which are represented in Figure 9. The SPWM gating signals for the next level are created on active switches S1 and S2, as shown in Figure 10.

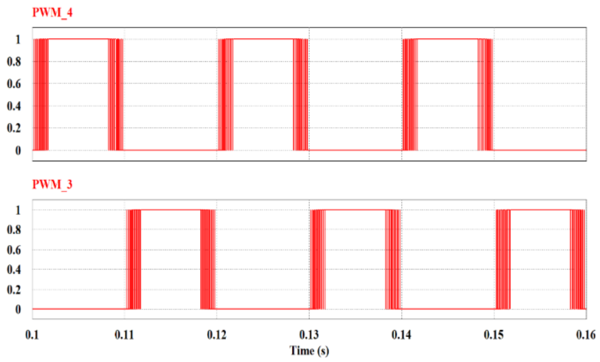

Figure 9. The SPWM gating signal S3 and S4.

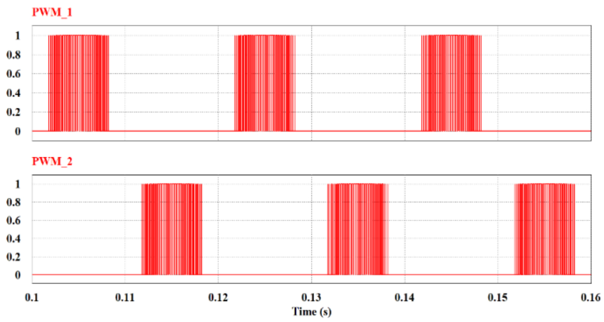

Figure 10. The SPWM gating signal S1 and S2.

The five-level output waveform of the simulation results in a structure of the proposed single-phase five-level inverter are shown in Fig 11. The fist magnitude voltage levels were at +400V, the second: +200V, the third: 0V, the fourth: −200V, and the last: −400V. The fundamental output waveform of five-level inverter is represented in Figure 12.

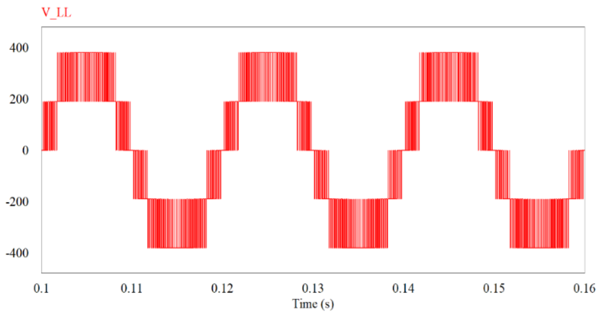

Figure 11. Five-level inverter output waveform.

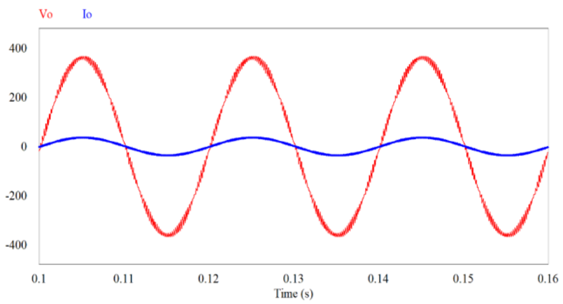

Figure 12. The current (blue) and Voltage (red) inverter output waveform.

Finally, the hardware implementation for the new proposed five-level inverter was conducted in the laboratory, and the experimental setup is shown in Figure 13. The minimum system microcontroller of the proposed control strategy implements a microcontroller, Arduino Mega 2560. Four modules IGBTs (SKM75GB123D) are used as active and passive power switches of the new proposed single-phase five-level inverter. The TLP 250 is used as an electric isolator for active switch S1 – S4. The single chip isolated power supply (B1212S-1W) is used for driver (TLP 250) and active switches S1-S4. The experimental results of the gating signals SPWM for the proposed five-level inverter are constructed on active switches S3 and S4, and they are represented in Figure 14. The gating signals for active switches S1 and S2 are shown in Figure 15. With the Comparison of simulation and hardware implementation results, it is shown that simulation and hardware implementation have the same switching pattern.

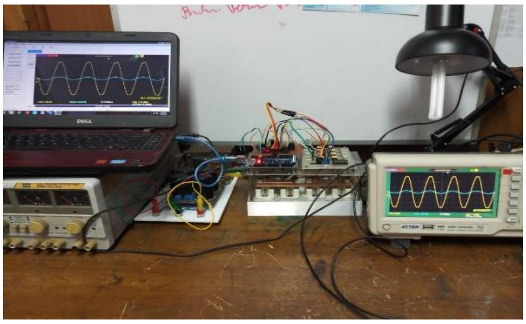
Figure 13. Hardware setup.

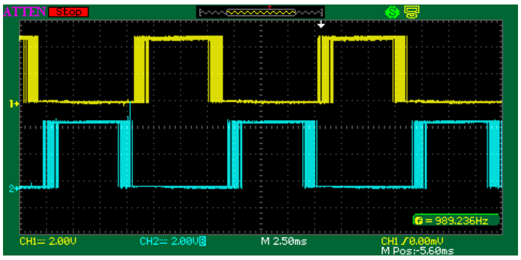

Figure 14. The gating signal S3 and S4

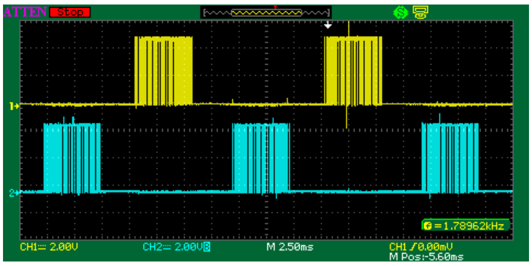

Figure 15. The gating signal S1 and S2.

The final tests for the hardware implementation of the proposed five-level inverter output waveform on each leg are shown in Figure 16. The magnitude voltage levels were at +400V, +200V, 0, −200V, and −400V. The proposed five-level inverter output waveform was filtered through an inductive filter of 2 mH, which is shown in Figure 17: (Yellow) for the fundamental voltage output waveform and (Blue) for the current output hardware.

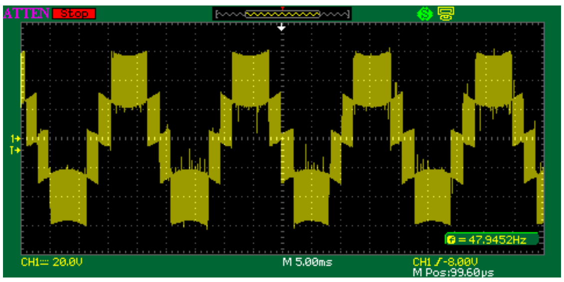

Figure 16. Five-level inverter output waveform.

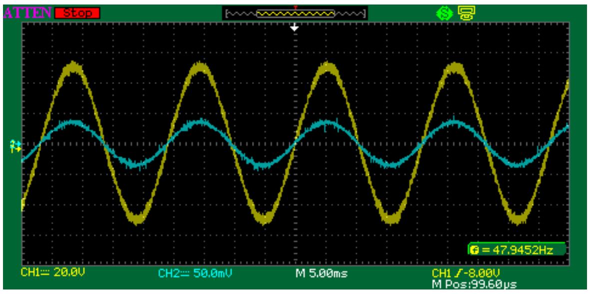

Figure 17. The current (blue) and voltage (yellow) inverter output waveform.

This verification of the simulation and hardware implementation showed that a new topology of a single-phase five-level inverter topology with a novel SPWM is very simple by controlling four switches.

4. CONCLUSION

The new proposed single-phase five-level inverter topology has four active switches and simple gating signal control. The results showed that this topology is simple, and it can be a good candidate for a renewable energy application converter. A novel sinusoidal pulse width modulation algorithm for the new single-phase five-level inverter topology had simplicity control. Also, the proposed topology can run well as a new single-phase five-level inverter with a level-phase shifted carrier for modulation strategy.

ACKNOWLEDGMENTS

The author would like to thank The Indonesian Ministry of Research, Technology and Higher Education (RISTEK-DIKTI) for funding under basic research for higher education (PDUPT 2019) scheme.

REFERENCES

[1] Arash Khoshkbar Sadigh, Seyed Hossein Hosseini, Mehran Sabahi, and Gevorg B. Gharehpetian, "Double Flying Capacitor Multicell Converter Based on Modified Phase-Shifted Pulsewidth Modulation, "*IEEE Transaction on Power Electronics*, Vol. 25, No. 6, pp. 1517-1526, 2010.

[2] Nasrudin A Rahim, Krismadinata Chaniago, and Jeyraj Selvaraj, "Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System, "*IEEE Transaction on Industrial Electronics*, Vol. 58, No. 6, pp. 2435-2443, 2011

[3] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, JoseI. Leon, and Leopoldo G. Franquelo, "Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge, "*IEEE Transaction on Power Electronics*, Vol. 27, No. 8, pp. 3505-3512, 2012.

[4] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters Topology, "*European Conference on Power Electronics and Applications*, 2005 , pp. 2296–2301.

[5] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter, "*IEEE Trans. Ind. Appl*, Vol. IA-17, No. 5, pp. 518–523, 1981.

[6] L. Lin, Y. Zou, Z. Wang, and H. Jin, "A simple neutral-point voltage balancing control method for three-level NPC PWM VSI inverters, "*in Proc. IEEE Int. Conf. Electr. Mach. Drives*, 2005, pp. 828–833.

[7] S. Guanchu, K. Lee, L. Xinchun, and L. Chongbo, "New neutral point balancing strategy for five-level diode clamped converters used in STATCOM of wind energy conversion systems, "*Proc. IEEE 6th Int. Power Electron. Motion Control Conf*, 2009, pp. 2354–2358.

[8] T. A. Meynard, and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," *in Proc. IEEE 23rd Annu. Power Electron. Spec. Conf*, 1992, pp. 397–403.

[9] L. H. Pratomo, F. D. Wijaya, and E. Firmansyah," A Simple Strategy of Controlling a Balanced Voltage Capacitor in Single Phase Five-Level Inverter, "*International Journal of Power Electronics and Drive System*, Vol 6, No. 1, pp. 160-167, 2015.

[10] J. M. Shen, L. H. Jou, C. J. Wu, and D. K. Wu," Five-Level Inverter for Renewable Power Generation System, "*IEEE Transactions on Energy Convertion*, Vol 28, No. 2, pp. 257-266, 2013.

[11] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, M. I. Gimenez," A new simplified multilevel inverter topology for DC-AC conversion, "*IEEE Transactions on Power Electronics*, Vol. 21, No. 5, pp. 1311-1319, 2006.

[12] L. H. Pratomo, "One Leg Control Strategy in Single-Phase Five-Level Inverter, "*The 2019 International Symposium on Electrical and Electronics Engineering*, 2019.

[13] Suroso, Daru Tri Nugroho, Abdullah Nur Azis, and Toshihiko Noguchi, "Simplified five-level voltage source inverter with level-phase shifted," *Indonesian Journal of Electrical Engineering and Computer Science*, Vol. 13, No. 2, pp. 461-468, 2019.

[14] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, Jose I. Leon, and Leopoldo G. Franquelo, "A Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge, "*IEEE Trans on Power Electronics,* Vol. 27, No. 8, pp. 3505-3512, 2012.

[15] Shalchi Alishah, R, Nazarpour, D. Hosseini, S.H and Sabahi, M, "Switched-diode structure for multilevel converter with reduced number of power electronic devices, "*Power Electronics, IET,* Vol.7, No.3, pp.648,656, 2014.

[16] Krishna Kumar Gupta, and Shailendra Jain, "Comprehensive review of a recently proposed multilevel inverter, "*IET Power Electron,* Vol. 7, No. 3, pp. 467–479, 2014.

[17] M. Aly, E. M. Ahmed and M. Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," *IEEE Transactions on Power Electronics*, Vol. 33, no. 11, pp. 9198-9208, 2018.

[18] Ebrahim Babaei, Mohammad Farhadi Kangarlu, and Farshid Najaty Mazgar, "Symmetric and asymmetric multilevel inverter topologies with reduced switching devices, "*Electric Power Systems Research*, Vol. 86, pp.122-130, 2012.

[19] Z. Li, P. Wang, Y. Li and F. Gao, "A Novel Single-Phase Five-Level Inverter with Coupled Inductors," *IEEE Transactions on Power Electronics,* Vol. 27, no. 6, pp. 2716-2725, 2012.

[20] G. Ceglia, V. Grau, V. Guzmán, C. Sánchez, F. Ibáñez, J. Walter, A. Millán, and M. I. Giménez," A New Multilevel Inverter Topology, "*Proceedings of the Fifth IEEE International Caracas Conference on Devices Circuits and Systems, Dominican Republic,* 2004, pp. 212-218.

[21] M Kavitha, A Arunkumar, N Gokulnath, S Arun, "New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources," *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE),* Vol. 2, Iss. 6, pp. 26-36, 2012.

[22] Harrish Pappu, G. Sasi Kumar, and Shiva Teja Manala, "An FPGA based new single phase five level inverter, "*International Conference on Energy, Communication, Data Analytics and Soft Computing* , 2017, pp. 1263-1267.

[23] H. Vu, Q. Tran and H. Lee, "A New Topology for Single-Phase Five-Level Voltage Source Inverter with Reduced Power Electronics Components," *2018 21st International Conference on Electrical Machines and Systems (ICEMS)*, Jeju, 2018, pp. 2194-2198.

[24] Samir Kouro , Jose I. Leon , Dimitri Vinnikov , and Leopoldo G. Franquelo, "Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology, "*IEEE Industrial Electronics Magazine,* Vol. 9, No. 1, pp. 47 – 61, 2015.

[25] M. Prodanović, and T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection, "*IEEE Transactions on Power Electronics*, Vol. 18, No. 1, pp. 373-380, 2003.

[26] T. C. Wang, Z. Ye, G. Sinha, and X. Yuan, "Output Filter Design for A Grid-Interconnected Three-Phase Inverter, "*IEEE 34th Annual Power Electronics Specialist Conference*, 2003, pp. 779-784.

[27] Rosalia Sinvula , Khaled M. Abo-Al-Ez , and Mohamed Tariq Kahn, "Total Harmonics Distortion (THD) with PV System Integration in Smart Grids: Case Study, "*International Conference on the Domestic Use of Energy,* 2019.

[28] R. O. Anurangi , Asanka S. Rodrigo , and Upuli Jayatunga, "Effects of high levels of harmonic penetration in distribution networks with photovoltaic inverters, "*IEEE International Conference on Industrial and Information Systems*, 2017, pp 1-6.

[29] S. Kandil , H. E. Farag , L. St. Hilaire , and E. Janssen, "A power quality monitor system for quantifying the effects of photovoltaic penetration on the grid, "*Canadian Conference on Electrical and Computer Engineering* , 2015, pp 237-241

BIOGRAPHY OF AUTHORS

L. Heru Pratomo was born in Ambarawa, Indonesia, in 1976. He received the B. Eng degree from Chatolic University, Semarang, Indonesia in 1994 and M. Eng degree from Bandung Institute of Technology, Bandung, Indonesia in 2004. He received Ph. D degree in electrical engineering from Gadjah Mada University, Jogjakarta, Indonesia in 2016. He has been a Lecturer and Researcher in the Electrical Engineering Department at Soegijapranata Catholic University, Semarang, Indonesia since 2000. Now. His current research is focused on multilevel inverter topology, active power filtering and PV-Grid Systems.