Indonesian Journal of Electrical Engineering and Informatics (IJEEI)
Vol. 4, No. 4, December 2016, pp. 225~239
ISSN: 2089-3272, DOI: 10.11591/ijeei.v4i4.237

Performance Evaluation of Three Different Inverter Configurations of DVR for Mitigation of Voltage Events

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Abstract

The voltage events namely voltage sags and voltage swells represent the most common, frequent and important power quality events in today's power system. Dynamic voltage restorer (DVR) is one of the key components used to mitigate the supply voltage quality disturbances in terms of voltage sags and swells in the distribution system. It consists of an energy storage unit, a voltage source inverter, a filter, a coupling transformer and the control system. This paper presents three different inverter configurations of dynamic voltage restorer (DVR) for mitigation of voltage events such as voltage sags and swells with sudden addition or removal of the nonlinear load. These three configurations are voltage source inverter based DVR (VSI-DVR), current source inverter based DVR (CSI-DVR) and impedance or Z-source inverter based DVR (ZSI-DVR). The d-q control technique is used to control the operation of the DVR. The response of ZSI-DVR for mitigation of voltage sags and swells are investigated and compared with VSI-DVR and CSI-DVR using MATLAB/SIMULINK environment.

Keywords: *power quality, voltage sag, voltage swell, dynamic voltage restorer, z-source inverter*

1. Introduction

In recent years, many researchers have given their focus on power quality. Discussing the quality of power is a complicated issue and is measured in terms of such things as line interruptions, voltage sags, voltage swells, flickers, harmonics, and distortion. However, among all disturbances, the voltage sags and voltage swells represents the most common, frequent and important power quality disturbances in today's power system [1,2]. Voltage sags are commonly known phenomenon in supply systems. A voltage dip (sag) is a disturbance where the RMS value of the line voltage is reduced for a period ranging from one-half cycle of the voltage to 500 ms [3]. A typical cause of voltage sags is the starting of large induction motors that normally draw 5 to 7 times their rated currents during start-up. Short circuits in the other branches of the supply are also a common origin of voltage sags. The sudden addition of a larger load and also loose or defective wiring can cause voltage sags [1,4]. Swell is opposite of sag. It is the short duration phenomenon of increase in RMS source voltage between 1.1 to 1.8 pu and duration of the event ranging from 0.5 cycles to 1 minutes. A voltage swell can occur due to a fault, energizing a larger capacitor bank, switching off of a heavy load [5-7]. Traditionally the passive filters are used for the enhancement of power quality. But currently new kinds of network configuration type custom power devices namely series connected Dynamic Voltage Restorer, shunt connected Distributed Static Compensator [8, 9] and series-shunt connected Unified Power Quality Conditioner [10, 11] have been commonly used due to their high performance to improve the controllability of power system. DVR is the key component used to compensate long duration voltage events such as voltage sags and voltage swells [12-15]. Generally, the DVRs consists of voltage source inverter based DVR (VSI-DVR), current source inverter based DVR (CSI-DVR) [16] and impedance source inverter based DVR (ZSI- DVR) [17-21]. The limitation of VSI-DVR is their buck (step-down) type output voltage characteristics thereby the maximum output voltage is limited by DC link voltage. The upper and lower IGBT switches of each leg of VSI cannot be fired on simultaneously, so a condition of shoot-through would appear and damage the IGBT switches. The shoot-through is a forbidden switching state for the VSI. The CSI-DVR is a boost type so the voltage at output level is greater than the DC voltage level. For the utilization where a large voltage is desirable, an additional DC-AC boost converter is required. The additional power conversion levels increase system cost and lower efficiency. At least one of the upper IGBT switches and one of the lower IGBT

Received August 18, 2016; Revised October 15, 2016; Accepted November 6, 2016

switches have to be fired on and maintain on at any time. Otherwise, an open circuit of the DC inductor would appear and damage the CSI. ZSI is an emerging type of converter which has unique characteristics so that it can overcome the disadvantages of VSI and CSI. The unique feature of the ZSI is that the output AC voltage can be any value between zero and infinity regardless of the DC voltage. That is, the ZSI is a buck-boost inverter that has a wide range of obtainable voltage. Unlike a VSI and CSI, the shoot-through state is not harmful and actually has been utilized in ZSI [17-21].In this paper, three different inverter configurations based on DVR such as VSI-DVR, CSI-DVR, and ZSI-DVR are discussed and compared. The VSI-DVR, CSI-DVR and ZSI-DVR is simulated using MATLAB\SIMULINK platform for mitigation of commonly occur voltage events such as voltage sags and voltage swells under nonlinear load condition. Comparative analysis of simulation results for the alleviation of voltage sags and swells under nonlinear load are also presented.

2. Research Method

DVR can be implemented by a three-phase voltage source, current source and Z-source inverters as depicted in Figure 1, Figure 2, and Figure 3. The structure of voltage sag/swell compensator contains a bank of three-single phase voltage source inverters. Each voltage source inverter group is associated with the network through three-phase an isolating transformer which provides isolation between the converters. Lf represents the inductance of each transformer as well as an additional interfacing inductance and is used to filter high-frequency components of injecting voltages.

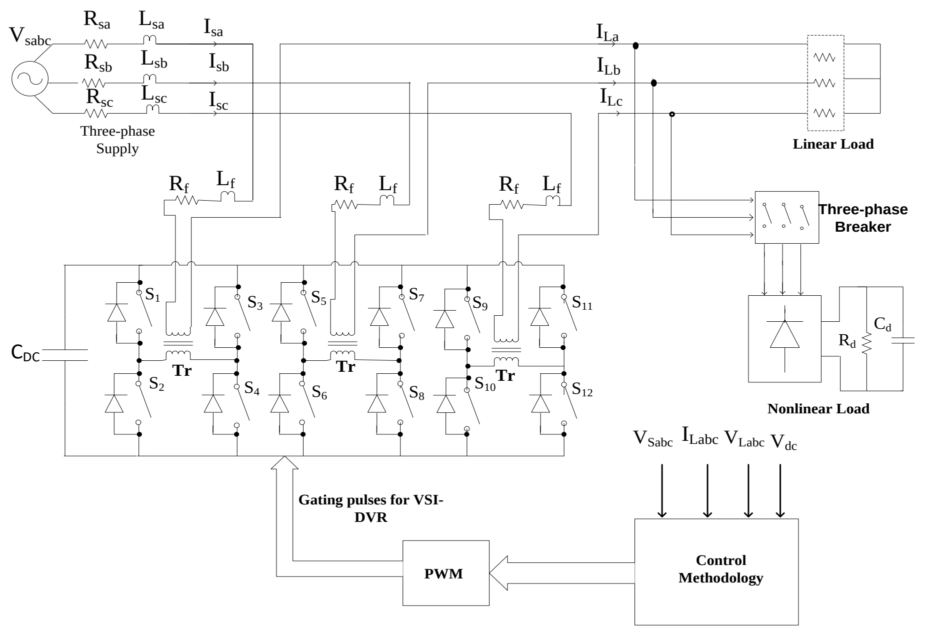

Figure 1. Schematic Diagram of Traditional VSI-DVR

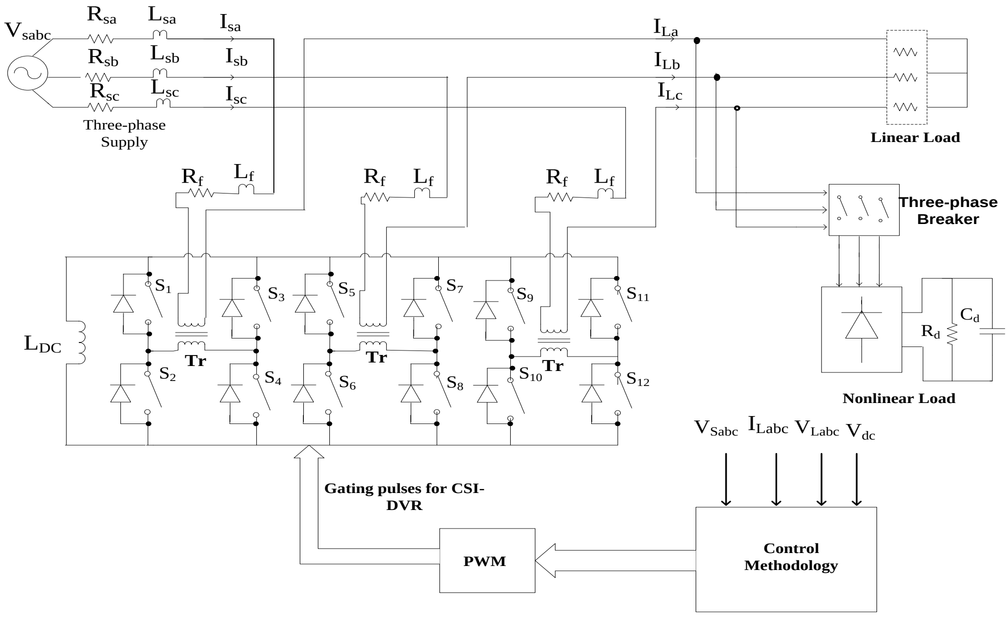

Figure 2. Schematic Diagram of Traditional CSI-DVR

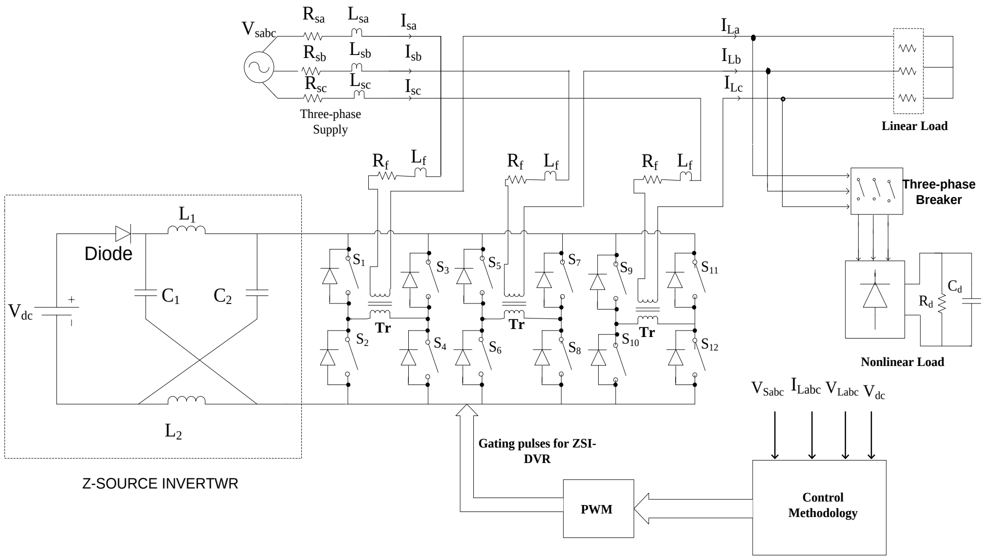

Figure 3. Schematic Diagram of Proposed ZSI-DVR

3. Voltage Source Inverter (VSI), Current Source Inverter (CSI) and Impedance Source Inverter (ZSI)

Figure 4 shows the 3-phase VSI. It is a DC-AC buck inverter with a capacitor on the DC side and works as a voltage source [22]. The usual converter switching devices are insulated gate bipolar transistor (IGBTs) and anti-parallel diodes to provide bidirectional current flow and unidirectional voltage blocking potential. A three-phase VSI basically has a six active modes and two zero modes. A zero state is produced when upper three or lower three devices are fired on as well as short-circuiting the output terminals. The two upper and lower IGBT switches of VSI cannot be fired on at the same period because a condition of shoot-through appears and damage the inverter.

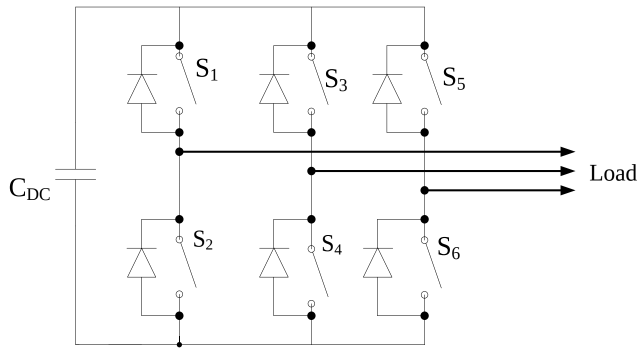

Figure 4. Basic Configuration of Voltage Source Inverter

VSI has the following limitations: (i) VSI is a DC-AC buck inverter. That means the obtained AC output voltage is lower than the DC bus voltage. For applications where a large range of AC output voltage is required, an additional DC-AC buck converter is used to obtain a desired AC output voltage. Due to additional converter stage increases a cost of the system and lower efficiency. (ii) shoot-through would appear and damage the devices.

Figure 5 shows the three-phase CSI. It is a DC-AC boost inverter with an inductance in the DC side.CSI has the following limitations:

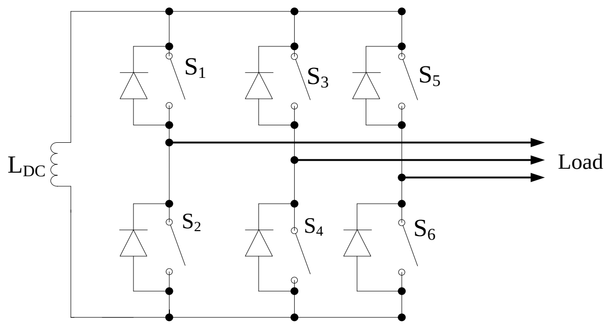

Figure 5. Basic Configuration of Current Source Inverter

(i) The CSI is a boost or step-up inverter so its voltage at output level is greater than the input DC voltage level. For the utilization where large voltage range is required an additional DC-AC step-down (step-up) inverter is used. The additional conversion levels increase system cost and lowers the efficiency. (ii) At least one of the upper devices and one of the lower devices have to be fired on and maintained on at any time because an open circuit across common inductor would appear and damage the inverter.

ZSIs are recently proposed inverter topologies that can perform both buck/boost function as a single unit. The VSI and CSI cannot provide such feature. The ZSI overcomes the above-mentioned problems of the VSI and CSI and provides a new concept of power conversion. The general configuration of three-phase ZSI is shown in Figure 6. The ZSI consists of two inductors L1 and L2 and capacitors C1 and C2 to form a unique impedance network to protect the IGBT switching devices when the devices are in a shoot-through state. Which is one of the important and significant feature of the ZSI.

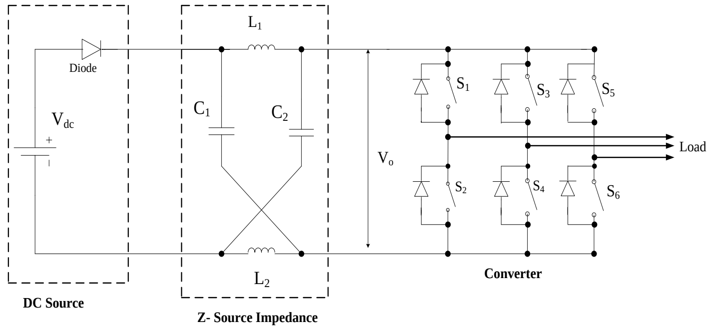

Figure 6. Basic Configuration of Z-Source Inverter

4. Operating Modes Of Z-Source Inverter

The ZSI has three operating modes: (i) normal mode (ii) zero-state mode (iii) shoot-through mode. Figure 7 shows active and zero states of ZSI.

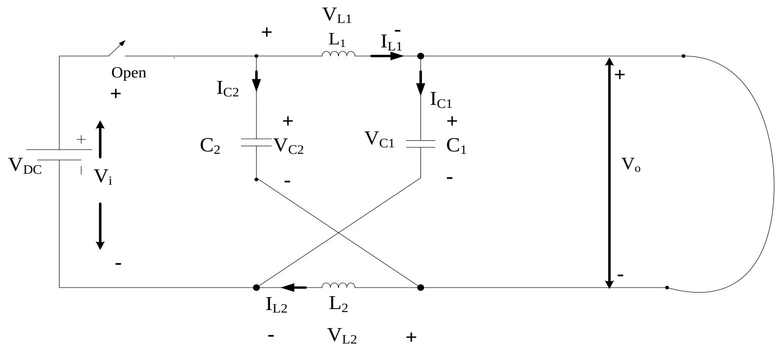

Figure 7. Active and Zero State of Z-Source Inverter

In these states diode is conducting at the DC-link side. The voltage across the inductors is

$$\left.\begin{aligned} V_L &= V_{DC} - V_C \\ V_C &= V_{DC} - V_L \end{aligned}\right\} \quad (1)$$

And Vi =VDC. The input voltage of the converter during active and zero states during interval t1 is

$$\begin{aligned} V_O &= V_C - V_L \\ V_O &= V_C - \left(V_{DC} - V_C\right) \\ V_O &= 2V_C - V_{DC} \end{aligned} \quad (2)$$

The mean voltage of the inductor over one switching interval t should be zero in steady state.

$$\int_{0}^{t=t_0+t_1} V_L dt = \int_{0}^{t=t_0+t_1} (V_{DC} - V_C) dt$$
$$V_L t = V_{DC}(t_0 + t_1) - V_C(t_0 + t_1) = 0$$
$$V_L t = V_{DC} t_0 + V_{DC} t_1 - V_C t_0 - V_C t_1 = 0$$
$$V_L t = (V_{DC} - V_C) t_0 + (V_{DC} - V_C) t_1 = 0$$
$$V_L t = V_C t_0 + V_{DC} t_1 - V_C t_1 = 0$$
$$V_L t = V_C (t_0 - t_1) + V_{DC} t_1 = 0$$
$$V_L = V_C \frac{(t_0 - t_1)}{t} + V_{DC} \frac{t_1}{t} = 0$$
$$\left(\frac{V_C}{V_{DC}}\right) = \left(\frac{t_1}{t_1 + t_0}\right) \quad (3)$$

Figure 8 shows the shoot-through mode of the ZSI where two switches of three legs turned on simultaneously. In a shoot-through mode, the diode at source side is off due to reverse bias and capacitors C1 and C2 charge the inductors L1 and L2.

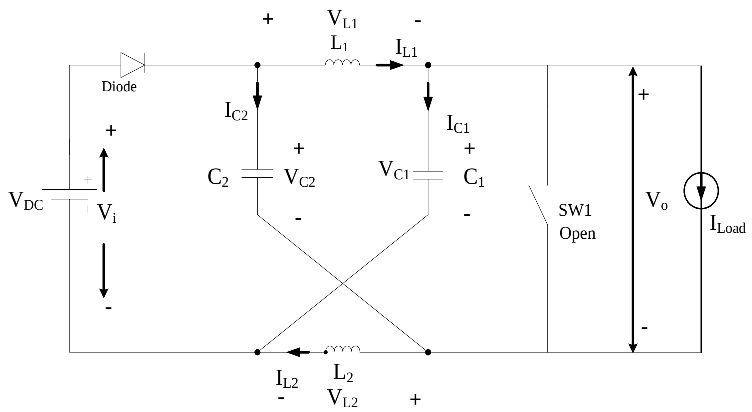

Figure 8. Shoot-Through Wtate of Z-Source Inverter

The DC-link voltage of the inverter is zero in shoot-through interval t0. The mean DC-link voltage across converter bridge during one switching cycle.

$$\int_0^{t=t_0+t_1} V_i dt = \int_0^{t=t_0+t_1} \left(2V_C - V_{DC}\right) dt$$
$$V_i t = 2V_C\left(t_0 + t_1\right) - V_{DC}\left(t_0 + t_1\right)$$
$$V_i t = 2V_C t_0 + 2V_C t_1 - V_{DC} t_0 - V_{DC} t_1$$
$$V_i t = \left(2V_C - V_{DC}\right)t_0 + \left(2V_C - V_{DC}\right)t_1$$
$$V_i t = t_0 * 0 + \left(2V_C - V_{DC}\right)t_1$$
$$V_i = \frac{t_1}{t}\left(2V_C - V_{DC}\right)$$
$$V_i = \frac{t_1}{t}\left[2\left(\frac{t_1}{t_1 + t_0}\right)V_{DC} - V_{DC}\right]$$
$$V_i = \frac{t_1}{t}\left[V_{DC}\left(\frac{t_1 + t_0}{t_1 - t_0}\right)\right]$$
$$V_i = V_{DC}\left(\frac{t_1}{t_1 - t_0}\right) \tag{4}$$

The peak DC-link Voltage across the inverter bridge is

$$V_0 = 2V_C - V_{DC}$$
$$V_0 = \left(\frac{t}{t_1 - t_0}\right)V_{DC}$$
$$V_0 = B_O V_{DC} \tag{5}$$

Where $B_0 = \left(\frac{t}{t_1 - t_0}\right) \geq 1$ is the boost factor resulting from the shoot-through state. The output peak phase voltage from the inverter can be expressed as

$$V_{AC} = M_i\left(\frac{V_0}{2}\right) \tag{6}$$

Where Mi is the modulation index. The voltage across the capacitors can be expressed as

$$V_C = \left(\frac{1 - {t_0}/{t}}{1 - {2t_0}/{t}}\right)V_{DC} \tag{7}$$

5. D-Q Control Technique

The control strategy plays a most important role in any distributed flexible AC transmission (D-FACTS) devices. The performance of DVR system solely depends on its control technique for generation of reference signals. In this paper d-q control technique is used to produce the reference signals. Figure 9 shows the d-q control strategy used to generate the reference signals of three inverter configurations of DVR.

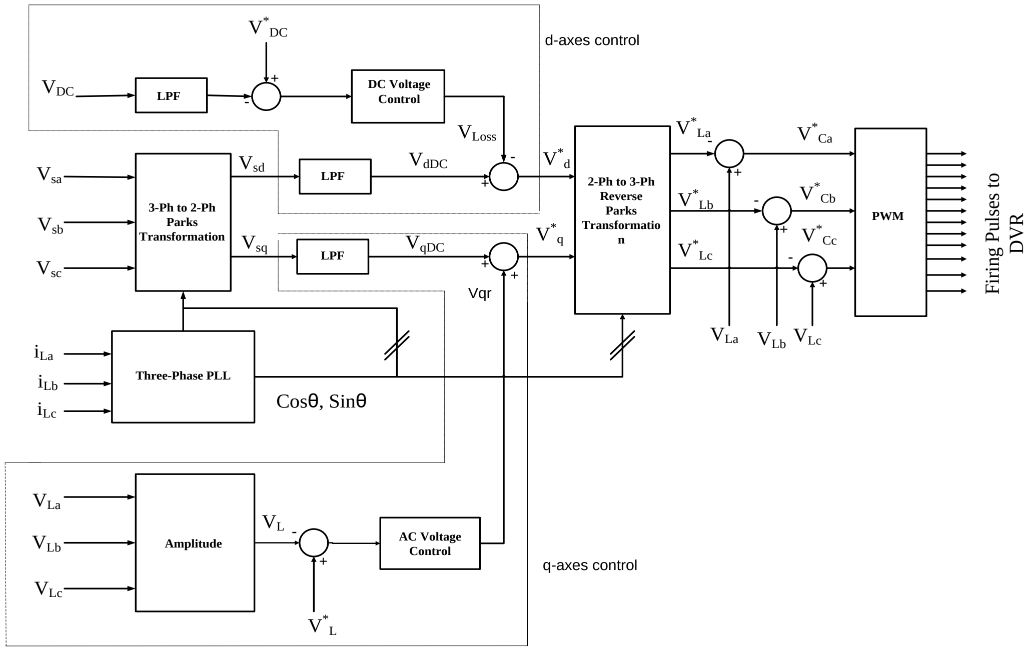

Figure 9. Block Diagram of D-Q Control Technique

The measured source voltages (Vs) are converted to rotating reference frame using the Parks transformation.

$$\begin{bmatrix} V_{Sd} \\ V_{sq} \\ V_{so} \end{bmatrix} = (2/3) \begin{bmatrix} \cos\theta & -\sin\theta & 0.5 \\ \cos\left(\theta - 120^0\right) & -\sin\left(\theta - 120^0\right) & 0.5 \\ \cos\left(\theta + 120^0\right) & -\sin\left(\theta + 120^0\right) & 0.5 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{8}$$

Low pass filters (LPFs) are used to mitigate the harmonics components of voltages. The components of voltages of direct and quadrature axes are

$$V_{sd} = V_{dDC} + V_{dAC} \tag{9}$$

$$V_{sq} = V_{qDC} + V_{qAC} \tag{10}$$

In order to maintain the DC bus voltage of the capacitor or inductor, a PI controller is used at the DC bus voltage of the DVR and output is considered as the voltage loss (VLoss).

$$V_{Loss(n)} = V_{Loss(n-1)} + K_{p1}\left(V_{de(n)} - V_{de(n-1)}\right) + K_{i1} V_{de(n)} \tag{11}$$

where $V_{de(n)} = V_{DC}^{*} - V_{DC(n)}$ is the error between the reference DC voltage (V_{DC}^{*}) and measured DC voltage (V_{DC}) at the nth sampling instant. KPI and Ki1 are the proportional and the integral gains of the PI controller. Therefore, reference direct axes (d-axes) load voltage is

$$V_{d}^{*} = V_{dDC} - V_{Loss} \tag{12}$$

The amplitude of the load terminal voltage (V_{L}) is controlled by its reference voltage (V_{L}^{*}) using another PI controller. The output of PI controller is considered as the reactive component of voltage (V_{qr}) for voltage regulation of load terminal voltage.

$$V_{qr(n)} = V_{qr(n-1)} + K_{p2}\left(V_{te(n)} - V_{te(n-1)}\right) + K_{i2}V_{te(n)} \tag{13}$$

where $V_{te(n)} = V_{L}^{*} - V_{L(n)}$ denotes the error between the reference load terminal voltage (V_{L}^{*}) and actual load terminal voltage ($V_{L(n)}$) amplitudes at the nth sampling instant. Kp2 and Ki2 are the proportional and the integral gains of the PI controller. The reference quadrature axes (q-axes) voltage is

$$V_{q}^{*} = V_{qDC} + V_{qr} \tag{14}$$

The reference load voltages ($V_{La}^{*}, V_{Lb}^{*}, V_{Lc}^{*}$) in abc frame are obtained from the reverse Parks transformation as in equation (15)

$$\begin{bmatrix} V_{La}^{*} \\ V_{Lb}^{*} \\ V_{Lc}^{*} \end{bmatrix} = \sqrt{\left(\tfrac{2}{3}\right)} \begin{Bmatrix} \cos(\omega t) & \sin(\omega t) \\ \cos\left(\omega t - \left(\tfrac{2\pi}{3}\right)\right) & \sin\left(\omega t - \left(\tfrac{2\pi}{3}\right)\right) \\ \cos\left(\omega t + \left(\tfrac{2\pi}{3}\right)\right) & \sin\left(\omega t + \left(\tfrac{2\pi}{3}\right)\right) \end{Bmatrix} \begin{bmatrix} V_{d}^{*} \\ V_{q}^{*} \end{bmatrix} \tag{15}$$

The errors between the sensed load voltages (V_{La}, V_{Lb}, V_{Lc}) and reference load voltages are used in the PWM controller to generate gate pulses for the VSC of the DVR.

6. Simulation of DVR

Figures 1-3 shows the three different inverter configurations of the test system used to carry out the simulation with the associated control technique. These DVR models are simulated under nonlinear load condition with simulation period 0.25 s.

7. Simulation Results and Discussion

In this section, simulation results of three different inverter topologies based on DVR for mitigation of voltage sag and swell under nonlinear load condition is presented. Load1 is considered as fixed resistive load (R-load) and load2 is considered as a nonlinear load. The nonlinear load is realized by three-phase diode-rectifier with R-C load. A three-phase breaker is used to control the connection of a nonlinear load to the distribution network. Initially, both the loads are connected to the network, but after a certain period of time load2 are switched on and off by opening the breaker. Due to the sudden change of the heavy load, voltage sag and swell occurs in the source voltage. The objective of the simulation is to study three different performance aspects: (i) Voltage sag and swell mitigation, by VSI-DVR under nonlinear load (ii) Voltage sag and swell mitigation by CSI-DVR under nonlinear load and (iii) Voltage sag and swell mitigation by ZSI-DVR under nonlinear load

7.1. Voltage Sag and Swell Mitigation by VSI-DVR under Nonlinear Load

Because of sudden addition or removal of the heavy nonlinear load, system encounters three-phase balanced voltage sag of magnitude 26% of the normal voltage which starts at t=0.01s and ends at t=0.05s and three-phase voltage swell of magnitude 18% of the normal voltage which starts at t=0.15s and ends at t=0.2s. For balanced voltage sag/swell, the supply voltage signal before compensation, the rms supply voltage, the compensation voltage, the load voltage after voltage sag/swell compensation and variation of DC link voltage are depicted in Figures 10(a)-(e). DVR does not produce any voltage during normal condition, but during voltage sag and swell condition, it generates voltage with required magnitude and polarity and injects to the system as depicted in Figure 10b. So that load voltage becomes sinusoidal as depicted in Figure 10c.

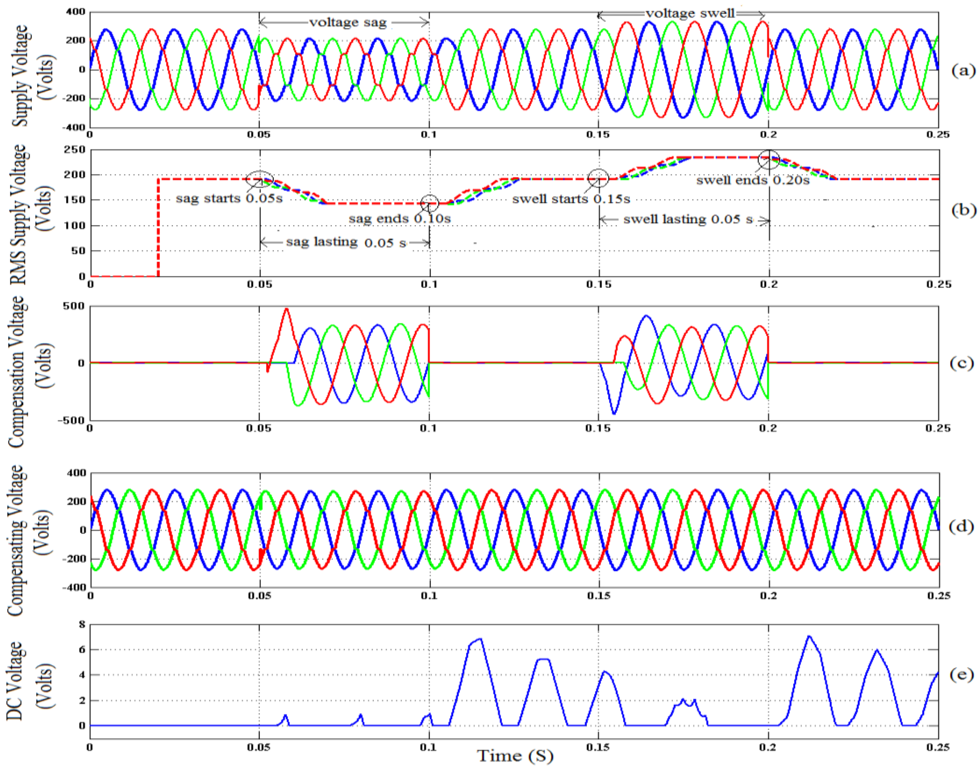

Figure 10. Simulation Results of VSI-DVR (a) Supply Voltage (b) RMS Supply Voltage (c) Injected Voltage of VSI-DVR (d) Load Voltage and (e) DC-link Voltage

Figure 11 depicts the load voltages under nonlinear load condition with VSI-DVR and without VSI-DVR. It can be observed from the waveform that, the system may experience sag/swell when VSI-DVR not connected to the system. During voltage sag and swell event, VSI-DVR is connected to the system and mitigates the effect of voltage sag and swell.

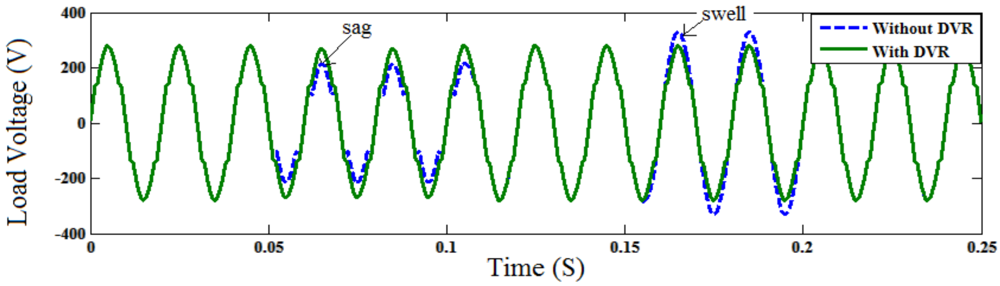

Figure 11. Load Voltage with and without VSI-DVR

7.2. Voltage Sag and Swell Mitigation by CSI-DVR under Nonlinear Load

In the period of a 0.05-0.10s heavy non-linear load is connected to the system by closing the breaker2. Due of sudden addition of non-linear load, the system may encounters voltage sag of magnitude 25% of the normal level and then the source voltage signal recovers to its normal levels. The system may also encounter a voltage swell of magnitude 14% of the normal voltage due to the sudden removal of a heavy non-linear load at 0.15-0.20s. For balanced voltage sag/swell, the supply voltage before compensation, the rms supply voltage, the DVR injecting missing voltage, the load voltage after voltage sag/swell compensation and variation of DC link voltage are depicted in Figures 12(a)-(e). CSI-DVR is activated only during sag or swell events and produces compensating voltage with required magnitude, frequency and polarity and injects to the three-phase distribution network as depicted in Figure 12b. It is clearly observed that VSI-DVR and CSI-DVR are injected the same amount of compensating voltage during sag and swell.

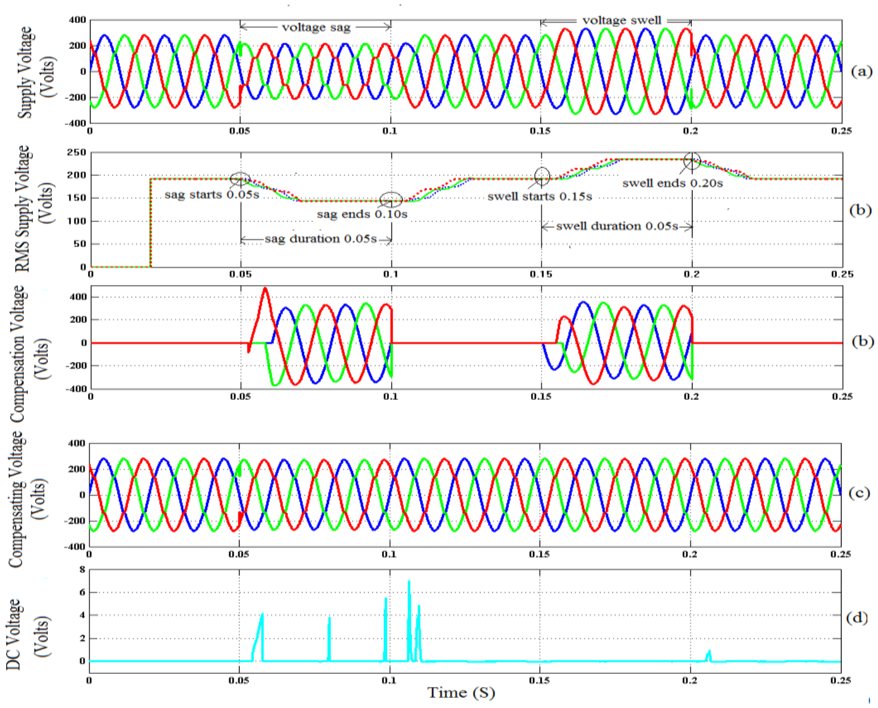

Figure 12. Simulation Results of CSI-DVR (a) Supply Voltage (b) RMS Supply Voltage (c) Injected Voltage of CSI-DVR (d) Load Voltage and (e) DC-link Voltage

Figure 13 depicts the load voltage under nonlinear load condition with CSI-DVR and without CSI-DVR. It can be observed from the waveform that, the system may experience voltage sag and swell when CSI-DVR not connected to the system. During voltage sag and swell event CSI-DVR is connected to the system and mitigates the effect of voltage sag and swell.

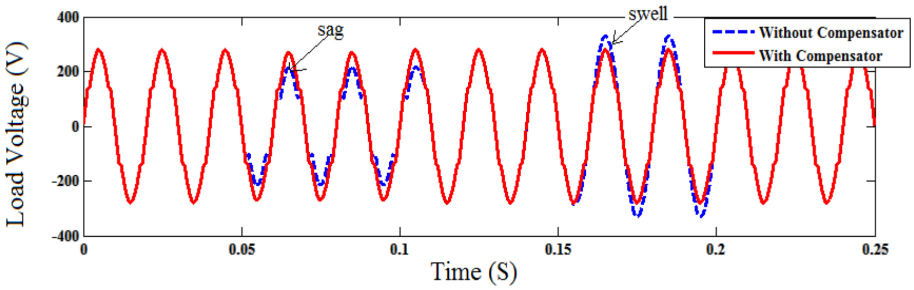

Figure 13. Load Voltage with and without CSI-DVR

7.2. Voltage Sag and Swell Mitigation by ZSI-DVR under Nonlinear Load

Figures 14(a)-(e) depicts the simulation results of ZSI-DVR with a nonlinear load. Due to load variation voltage sag of magnitude 24% of the normal voltage which starts at t=0.01s and ends at t=0.05s and three-phase voltage swell of magnitude 14% of the normal voltage from 0.15-0.2s occurs in the distribution system. For balanced voltage sag/swell, the supply voltage signal, the RMS supply voltage, the compensation voltage, the load voltage and variation of DC link voltage are depicted in Figures 14(a)- (e). DVR does not produce any voltage during normal condition, but during voltage sag and swell condition, it generates voltage with required magnitude and polarity and injects to the network and keeps the load voltage at the desired level as in the normal operating condition.

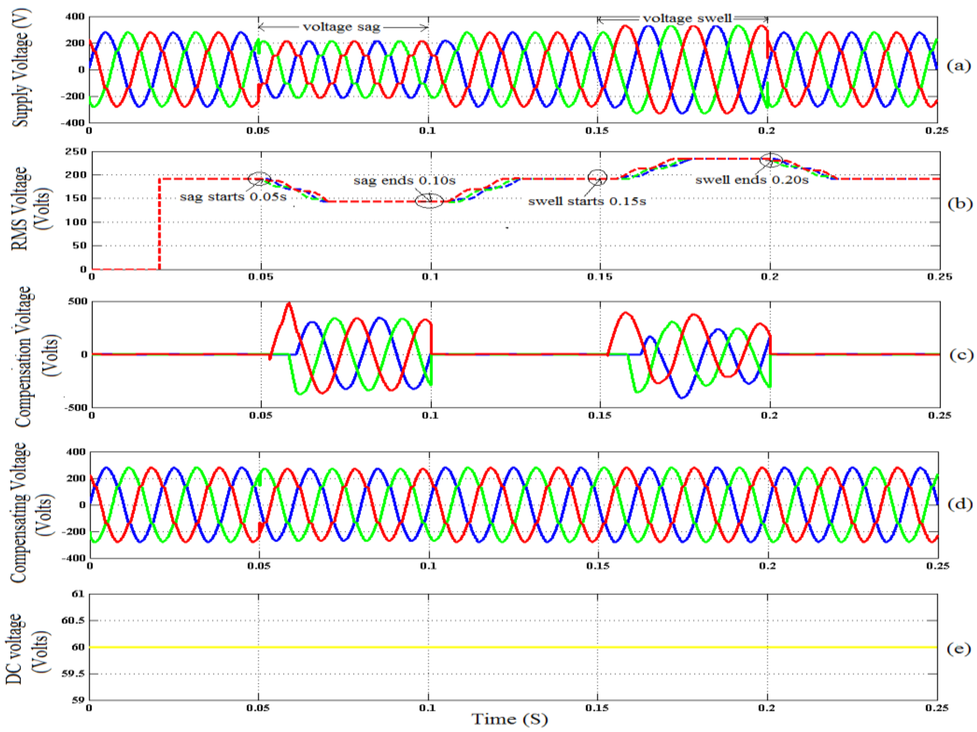

Figure 14. Simulation Results of ZSI-DVR (a) Supply Voltage (b) RMS Supply Voltage (c) Injected Voltage of ZSI-DVR (d) Load Voltage and (e) DC-link Voltage

The first simulation contains without ZSI-DVR and it is observed that, the system experience voltage sag and swell. The second simulation is carried with ZSI-DVR. When ZSI-DVR is connected to the system, it produces the proper amount of compensating voltage so that voltage sag and swell is completely eliminated as shown in Figure 15.

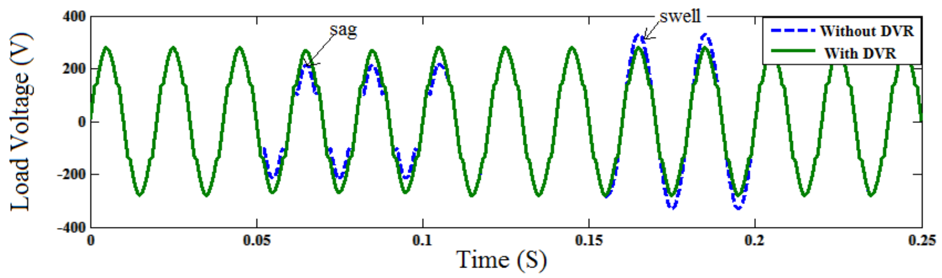

Figure 15. Load Voltage with and without ZSI-DVR

The ZSI based DVR mitigates serious and deepest voltage sags compared to VSI and CSI based DVR as shown in Table 1. Table 2 shows the comparative analysis of three configurations of DVR.

Table 1. Measured Voltage Sag/Swell By VSI-DVR, CSI-DVR AND ZSI-DVR

Inverter Configuration	Supply Voltage Events	
	Voltage Sag	Voltage swell
VSI-DVR	26%	18%
CSI-DVR	25%	14%
ZSI-DVR	24.8%	14%

Figure 17 depicts a chartable representation of measured voltage sag and swell mitigation under VSI-DVR, CSI-DVR, and ZSI-DVR. ZSI-DVR mitigates the deepest voltage sag (24.8%) compared to VSI-DVR (26%) and CSI-DVR (25%).

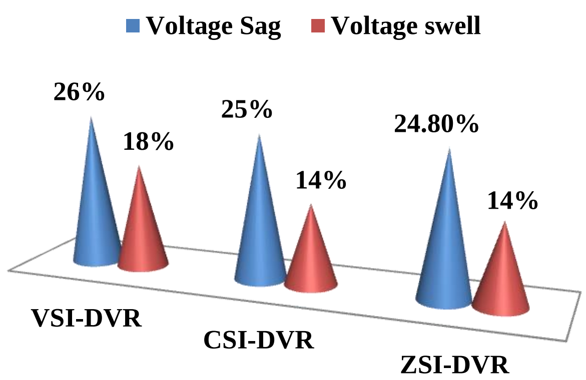

Figure 17. Measured Chat for Voltage Sag/Swell by VSI-DVR, CSI-DVR and ZSI-DVR

Table 2. Comparative Analysis of VSI, CSI AND ZSI

Voltage Source Inverter (VSI)	Current Source Inverter (CSI)	Impedance Source Inverter (ZSI)
1. It acts as a low impedance voltage source because capacitor used in the DC-link	1. It acts as a high impedance constant current source because inductor used in the DC-link	1. It acts as a constant high impedance voltage source because capacitor and inductor used in the DC-link
2. Used in only buck operation of inverter.	2. Used in only boost operation of inverter.	2. Used both buck and boost operation of inverter.
3. Main circuit cannot be interchangeable.	3. Main circuit cannot be interchangeable.	3. Main circuits are interchangeable.
4. Power loss is high so low efficiency.	4. Power loss is high so low efficiency.	4. Power loss should be low so higher efficiency.
5. It has a considerable amount of harmonic distortion	5. It has a considerable amount of harmonic distortion	5. Harmonic distortion is low
6. Good voltage sag and swell mitigation capability.	6. Good voltage sag and swell mitigation capability.	6. Excellent voltage sag and swell mitigation capability.
7. Injected voltage is low compare to ZSI during voltage sag and swell	7. Injected voltage is also low compare to ZSI during voltage sag and swell	7. Injected voltage is high compare to VSI and CSI during voltage sag and swell

4. Conclusion

In this work three different inverter topologies such as VSI-DVR, CSI-DVR and ZSI-DVR are tested using MATLAB/SIMULINK platform under nonlinear load condition for mitigation of supply voltage disturbances like voltage sags and swells in a distribution system. It is found that ZSI-DVR shows a superior performance to mitigate the most significant power quality events such as voltage sags and swells in the supply voltage compared to VSI-DVR and CSI-DVR.

References

[1] M.P Kazmierkowski, R. Krishnan, F Blaabjerg. Control in Power electronics selected problems. New York: Academic press. 2002: 462-482.

[2] P.R Ramesh Babu, P. K Dash, S. K Swain, S. Sivanagaraju. A New Fast Discrete S-Transform and Decision Tree for the Classification and Monitoring of Power Quality Disturbance Waveforms. *International Transactions on Electrical Energy Systems*. 2014; .24: 1279-1300.

[3] M.H Moradi, Y Mohammadi. A New Current-Based Method for Voltage Sag Source Location Using Directional Overcurrent Relay Information. *European Transactions on Electrical Power*. 2013; 23: 170-181.

[4] R. Kapoor, R. Gupta. Fuzzy Lattice Based Technique for Classification of Power Quality Disturbances. *European Transactions on Electrical Power*. 2012; 22: 1053-1064.

[5] C. Venkatesh, S.D.V.S.S Siva, M. Sydulu. Mitigation of Voltage Sag/Swell Using Peak Detector Based Pulse Width Modulation Switched Autotransformer. *Electric Power Components and Systems*. 2011; 39: 1117–1133.

[6] E.F Fuchs, M.A.S Masoum. Power Quality in Power Systems and Electrical Machines. Perth: WA. 2008.

[7] M.R Alam, K.M Muttaqi, A. Bouzerdoum. Characterizing Voltage Sags and Swells Using Three-Phase Voltage Ellipse Parameters. *IEEE Transaction on Industry Application*. 2015; 51: 2780-2790.

[8] B. Singh, S.J Arya, P. Verma. An Implementation of Double-Frequency Oscillation Cancellation Technique in Control of DSTATCOM. *International Transactions on Electrical Energy Systems*. 2014; 24: 796–807.

[9] C.K Sundarabalan, K Selvi. PEM Fuel Cell Supported Distribution Static Compensator for Power Quality Enhancement in Three-Phase Four-Wire Distribution System. *International Journal of Hydrogen Energy*. 2014; 39: 19051-19066.

[10] Y. Bouzelata, E. Kurt, R. Chenni, N. Altın. Design and Simulation of a Unified Power Quality Conditioner Fed by Solar Energy. *International Journal of Hydrogen Energy*. 2015; 40: 15267-15277.

[11] L. F. C Monteiro, M. Aredes, C. Couto, J.L Afonso. Control Algorithms for a Unified Power Quality Conditioner Based on Three-Level Converters. *International Transactions on Electrical Energy Systems*. 2015; 25: 2394-2411.

[12] C.K Sundarabalan, K. Selvi. Compensation of Voltage Disturbances using PEMFC Supported Dynamic Voltage Restorer. *Electrical Power and Energy Systems*. 2015; 71: 77-92.

[13] A.K Sadigh, K.M Smedley. Fast and Precise Voltage Sag Detection Method for Dynamic Voltage Restorer (DVR) Application. *Electric Power Systems Research*. 2016; 130: 192–207.

[14] S.A Rahman, P.A Janakiraman, P. Somasundaram. Voltage Sag and Swell Mitigation Based on Modulated Carrier PWM. *Electrical Power and Energy Systems*. 2015; 66: 78–85.

[15] R. Nittala, A.M Parimi, K.U Rao. *Comparing the Performance of IDVR for Mitigating Voltage Sag and Harmonics with VSI and CSI as Its Building Blocks.* IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems, Kozhikode. 2015: 1-5.
[16] M.R Banaei, A.Z Dehghanzadeh. *DVR Based Cascaded Multilevel Z Source Inverter*. IEEE International Conference on Power and Energy. 2010: 51-56.
[17] M. Rajkumar, R.P Usha, S.R Reddy. *Modeling and Simulation of ZSI based DVR for Voltage Compensation*. International Conference on Computer, Communication and Electrical Technology. 2011; 346-351.
[18] M. Balamurugan, T.S Sivakumaran, M.A. Devi. *Voltage Sag/Swell Compensation Using Z-source Inverter DVR based on FUZZY Controller*. IEEE International Conference on Emerging Trends in Computing, Communication and Nanotechnology. 2013: 648-653.
[19] P.H Zope, A Somkuwar. Design and Simualtion of Single-phase Z-Source Inverter for Utility Interface*. International Journal of Electrical Engineering and Technology*. 2012; 1: 127-143.
[20] Y. Tang, S. Xie, C. Zhang. An Improved Z-Source Inverter*. IEEE Transactions on Power Electronics*. 2011; 26: 3865-3868.
[21] V. Saravanan, R. Ramanujam, M. Arumugam. Novel Improved Three Level Z-source Inverter. *Australian Journal of Electrical and Electronics Engineering.* 2015; 12: 133-140.
[22] M.M Antonio. Power Quality Mitigation Techniques in a Distributed Environment. Springer-Verlag London Limited. 2007.