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MLI Power Topologies and Voltage Eminence: An Exploratory Review

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Abstract

Due to their performances and inherent edges, particularly in medium-voltage and dynamic applications, multilevel inverters have received associate degree increasing attention in universe industrial applications. This paper deals with a review of the most structure electrical converter topologies additionally their commonest derived and hybrid structures quoted in previous analysis works. It additionally encompasses associate degree investigation on voltage harmonic elimination and THD estimation. For that reason, the paper summarizes the foremost relevant modulation techniques used to date to boost the output voltage quality. Theoretical formulas elicited within the literature, for calculating the output voltage THD higher and lower bounds area unit reportable and verified by adequate simulations.

Keywords*: multilevel inverter topologies, modulation, control algorithms, voltage quality bounds, Total Harmonic Distortion (THD)*

1. Introduction

Multilevel inverters square measure DC-AC static power converters exhibiting at their output terminals quite two-level voltage waveforms. Today they notice increasing attention especially for medium-voltage and high-voltage applications [1, 2]. Within the middle 1970's, Baker and Bannister have proposed the primary structure electrical converter [3]. It consists of series connected single part H-bridges. Later, Nabae et al. developed another structure electrical converter known as 3L-NPC (Neutral point Clamped diodes) [4]. In such topology, several diodes guarantee levels construction of output voltage by linking electrical phenomenon sources to switches. Following the NPC, a Flying Capacitors topology (FLC) was planned by putt clamping capacitors rather than diodes [5]. As a consequence, cascaded H-bridge, authority and FLC square measure the basic and most used structure inverters. After that, multitude of derived and hybrid structure topologies were introduced [6-16]. However, they still on the shadow of the foremost structure configurations antecedently expressed. The most industrial structure topologies square measure the three-level authority (3L-NPC), the cascaded H-bridge (MLCHB), and the four-level flying capacitors (4L-FLC) [17]. Typically, structure topologies are accustomed overcome the constraints of standard two-level inverters.

Particularly, the voltage stress on shift devices is decreased by fixing series power switches. The total harmonic distortion is reduced by adding steps or levels in the output voltage wave form fitted with the curved reference. In apply; this is often achieved by multiplying the number of DC sources and additionally by considering their terminals as positions to be switched [18]. Multilevel inverters options have many different promising advantages over 2 level topologies such as: i) the possibility to beat the matter associated with the utmost voltage drop of the most power semiconductors. ii) Transformer- less electrical converter design fascinating in renewable energy applications [19]. iii) Reduction of the common mode voltage that causes inherent damages of the bearings. iv) High resolution of the output waveforms [20, 21]. Therefore, the voltage adjustment is swish which reduces the strain on the load; otherwise the voltage in standard electrical converter varies between 2 values. The rating of passive filters, generally necessary to limit these stresses, may be additionally reduced. Consequently, the system wins additional dynamic and permits quicker regulation. v) reduced magnetism interference problems [22]. Multilevel inverters applications cowl in the main the variable speed space as motors drives [23-26], pumps [27], conveyors [27, 28] and electrical traction [29-31]. Construction inverters are also used for wattage learning as voltage rectifier, static compensator

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(STATCOM), Back to Back inverter connected to the network [32-35]. Recently, they are related to renewable energy systems in electrical phenomenon applications and alternative energy [22, 36-39]. Thanks to the development of semiconductors dedicated to high power, significantly IGBTs at three.3 kV, 4.5 kV and 6.5 kV, the power ranges associated to structure inverters were significantly extended to medium and high voltages (2-13 kV). Regarding management algorithms, the oftentimes used techniques are Selective Harmonic Elimination (SHE) and Pulse width modulation (PWM) [40]. Advanced strategies developed thereafter area unit enhancements of these on top of. PWM based techniques area unit most relevant in industrial field including multi carriers and house vector modulation. With those techniques, we will cut back shift losses and win a coffee total harmonic distortion, so better voltage quality.

Elsewhere, this review paper is increased by introducing Ruderman works [41-44]. These latter permits the estimation of the entire harmonic distortion supported a time study rather than frequency domain. This will remedy THD's estimation errors particularly for prime frequency switching. Contrary to what's common, Ruderman incontestable that, just in case of three-phase balanced load with isolated neutral, THDs of each line and section voltages area unit the same. He additionally established intuitive straightforward hyperbolic formulas which can be used as a relevancy calculate reliable structure convertor voltage THDs. To our information, this fascinating approach is that the initial time addressed in a review paper.

The present paper is organized in an exceedingly means in order that it could function reference for electrical converter specialists similarly as for fresh introduced within the field. Torture the introduction and also the conclusion, section a pair of offers a general overview of the most structure topologies mentioned in the literature (H-Bridge, NPC, FC) with their operative principle and associated mathematical models. In section 3, a number of common derived configurations area unit reported. Examples of hybrid structures area unit elaborated in section four. Finally, section five is dedicated to the output voltage quality analysis.

2. Multilevel Inverters Main Topologies

2.1. Cascaded full bridge inverter

Cascaded full bridge construction inverters also are referred to as series connected H-bridge or cascaded H-bridge. It consists in connecting serial single-phase H-bridges. Every single phase inverter may be a full partial cell fashioned by four bidirectional switches (MOSFET, IGBT or GTO + free-wheel diode connected in anti parallel) and a DC voltage supply E. The output voltage generated by associate degree H-bridge has 3 levels (−E, 0, E). The DC power provides should be specific or dedicated to every single-phase bridge and electrically isolated from one another [45]. This permits overcoming problems concerning charge leveling of the DC link capacitors as in bureau topologies and prevents unwanted short circuits across the capacitors.

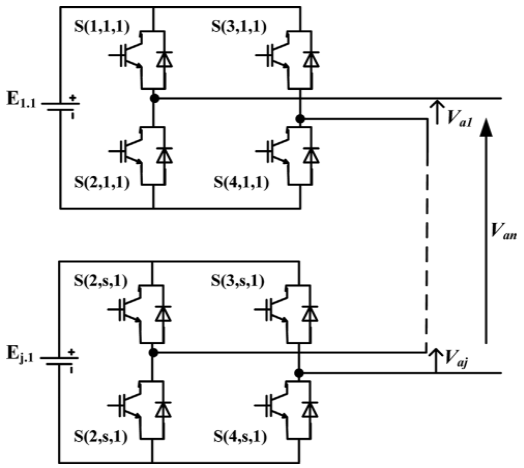

Figure 1. Topology of an H-bridge arm composed by S cells connected in series.

The generalized topology of associate degree m level H-Bridge arm is shown in Figure 1. The language of this structure is as follows:

a. The switch S(i, j, k) is that the ith switch of the jth cell belonging to the kth part.
b. The DC supply Ej,k is that the voltage supply supply the jth cell of the kth part.
c. (Vaj, Vbj, Vcj) area unit the output voltages of the jth cell respectively of the primary, second and third part.
d. (Van, Vbn, Vcn) area unit severally the part voltages of the first, second and third arm.
e. S represents the cell range.

The stepped voltage undulation consists by m levels which depends on the DC sources range such m = 2S+1. Thus, regardless of the variety of cascaded construction inverter is, the output voltage levels range is often odd (3, 5, 7, 11...). The various H cells area unit connected in series so the ensuing voltage of associate degree arm is adequate to the aid of all voltages generated by every cell:

$$V_{an} = \sum_{i=1}^{s} V_{ai} \quad (1)$$

For S = 2, the three phase and line output voltages can be expressed as follows:

$$\begin{cases} V_{an} = E \times \sum_{j=1}^{s}[S(1,j,1) + S(4,j,1) - 1] \\ V_{bn} = E \times \sum_{j=1}^{s}[S(1,j,2) + S(4,j,2) - 1] \\ V_{cn} = E \times \sum_{j=1}^{s}[S(1,j,3) + S(4,j,3) - 1] \end{cases} \quad (2)$$

$$\begin{cases} U_{ab} = E \times \sum_{j=1}^{s}\left[\left(S(1,j,1) + S(4,j,1)\right) - \left(S(1,j,2) + S(4,j,2)\right)\right] \\ U_{bc} = E \times \sum_{j=1}^{s}[(S(1,j,2) + S(4,j,2)) - (S(1,j,3) + S(4,j,3))] \\ U_{ca} = E \times \sum_{j=1}^{s}[(S(1,j,3) + S(4,j,3)) - (S(1,j,1) + S(4,j,1))] \end{cases} \quad (3)$$

2.2. Cascaded full bridge inverter

The first structure, specifically the three-level government agency, was first introduced by Nabae within the 80's [4]. The NPC inverter is made by victimization many continuous buses having equal capacities fed by just one DC power offer as depicted in Figure 2. The presence of clamping diodes links each combine of switches to a bus for the aim to make voltage levels inside their shift order. These diodes also guarantee current changeableness. For Associate in nursing m-level government agency electrical converter, the quantity of capacitors, power switches and diodes required for every leg are defined as:

1. Number of capacitors: C = m−1
2. Number of power switches: K = 2(m−1)
3. Number of clamping diodes: D = 2(m−2).

It ought to be noted that every few change devices (S (1, j), S'(1, j)) commutates in a very complementary method. The output voltage Vao generated by the primary leg of the converter are often expressed by:

$$V_{a0} = \pm K' \frac{E}{m-1}$$
$$K \in \left[0, \frac{m-1}{2}\right] \quad (4)$$

Sah is that the shift sequence of the primary leg a. The switches S (1, j) and S'(1, j) change by reversal within the sequence given by equation (5). As example, for h = one (first shift sequence), Sa1 = S (1, 1) + S (1, 2) + S (1, 3) + S (1, 4), which gives Vao = E/2.

$$S_{ah} = \sum_{j=K}^{m-1} S(1,j) - \sum_{j=1}^{K-1} S'(1,j) \qquad \text{where } h \in [0.m] \quad (5)$$

Regarding the possible switching states, the corresponding output voltage, referred to the middle point o for each leg, can thereafter be expressed as:

$$\begin{aligned} V_{ao} &= (2 \times \sum_{j=1}^{m-1} S(1,j) - (m-1)) \frac{E}{2(m-1)} \\ V_{bo} &= (2 \times \sum_{j=1}^{m-1} S(2,j) - (m-1)) \frac{E}{2(m-1)} \\ V_{co} &= (2 \times \sum_{j=1}^{m-1} S(3,j) - (m-1)) \frac{E}{2(m-1)} \end{aligned} \quad (6)$$

Expressions of phase to neutral and line to line output voltages are given by (7) and (8) respectively:

$$\begin{cases} V_{an} = \frac{E}{3(m-1)} [2 \times \sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j)] \\ V_{bn} = \frac{E}{3(m-1)} [- \sum_{j=1}^{m-1} S(1,j) + (2 \times \sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j))] \\ V_{cn} = \frac{E}{3(m-1)} (- \sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j) + (2 \times \sum_{j=1}^{m-1} S(3,j))] \end{cases} \quad (7)$$

$$\begin{cases} U_{ab} = (\sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j)) \frac{E}{(m-1)} \\ U_{bc} = (\sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j)) \frac{E}{(m-1)} \\ U_{ca} = (\sum_{j=1}^{m-1} S(3,j) - \sum_{j=1}^{m-1} S(1,j)) \frac{E}{(m-1)} \end{cases} \quad (8)$$

2.3. Flying Capacitors

This topology was planned by T. Meynard and H. Foch in 1992 [5]. it's conjointly called nest cell convertor because it's divided into many cells nested within every other. Clamping capacitors is additionally another name which will be found within the literature [46]. A cell consists of a electrical device and a complementary try of switches, as portrayed in Figure 3. This electrical converter alleviates the clamping diodes problems by substituting them with capacitors. These latter are connected in series with the DC power provide as a result of the absence of diodes makes not possible to attach directly the load to the required DC voltage. The 'clamping capacitors' help to stay constant the drop between busses to which they're connected [47]. For Associate in nursing m-level flying capacitors electrical converter the quantity of capacitors, power switches, and commutation cells required for every leg are outlined as:

a. Number of capacitors: C = m−1
b. Number of power switches: K = 2(m−1)
c. Number of commutation cells: D = m.

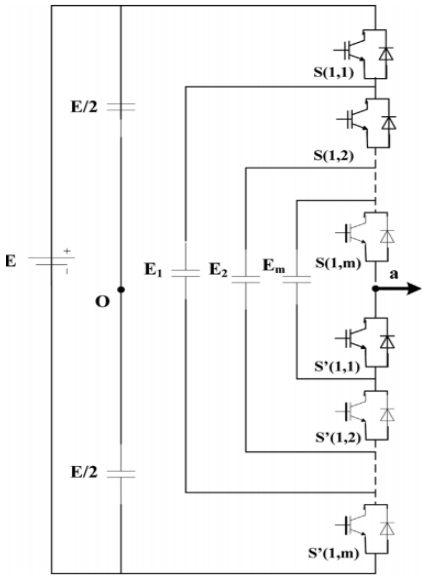

Figure 3. Topology of an m-level Flying Capacitors leg.

Converter typical voltages are:

$$\begin{cases} V_{ao} = -\frac{E}{2} + \sum_{j=1}^{m-1} S(1,j)\frac{E}{(m-1)} \\ V_{bo} = -\frac{E}{2} + \sum_{j=1}^{m-1} S(2,j)\frac{E}{(m-1)} \\ V_{co} = -\frac{E}{2} + \sum_{j=1}^{m-1} S(3,j)\frac{E}{(m-1)} \end{cases} \quad (9)$$

$$\begin{cases} U_{ab} = (\sum_{j=1}^{m-1} S(1,j) - \sum_{j=1}^{m-1} S(2,j))\frac{E}{(m-1)} \\ U_{bc} = (\sum_{j=1}^{m-1} S(2,j) - \sum_{j=1}^{m-1} S(3,j))\frac{E}{(m-1)} \\ U_{ca} = (\sum_{j=1}^{m-1} S(3,j) - \sum_{j=1}^{m-1} S(1,j))\frac{E}{(m-1)} \end{cases} \quad (10)$$

3. Multilevel Inverters Derived Structure

3.1. H-Bridge derived structures

To reduce the amount of large DC sources, new categories of cascaded H-bridge were projected. The uneven full bridge inverters were another. They need an equivalent configuration because the cascaded symmetrical inverters except that continuous sources values don't seem to be equals however multiples of every other's [6]. Generally, the DC sources are multiples of 2 (2E, 4E...), Figure 4. Thus, the number of output voltage levels will increase up to 2(n +1) −1.

Furthermore, per [20], AN H-bridge electrical converter can simply operate with only 1 isolated DC power source; the other sources could also be replaced by capacitors. Consequently, this topology needs a selected management strategy to regulate the voltage across the capacitors [8]. Modular construction convertor (MMC) is additionally AN innovative structure within the HVDC family that plan is inspired from cascaded H-bridge electrical converter. This topology provides output waves with high range of levels that can be extendible to any desired one with adjustable AC voltage magnitude [9, 10]. Siemens integrated the primary MMC in wattage grid application as HVDC and. Each arm is built out of sub modules connected in series.

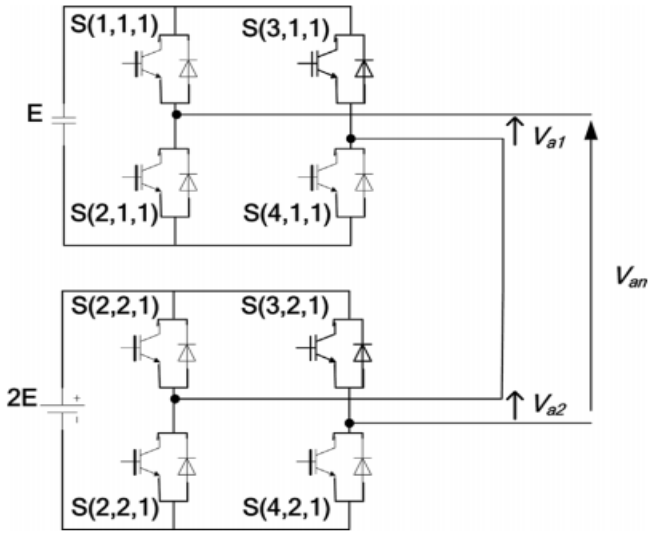

Figure 4. Topology of an asymmetric H-Bridge arm.

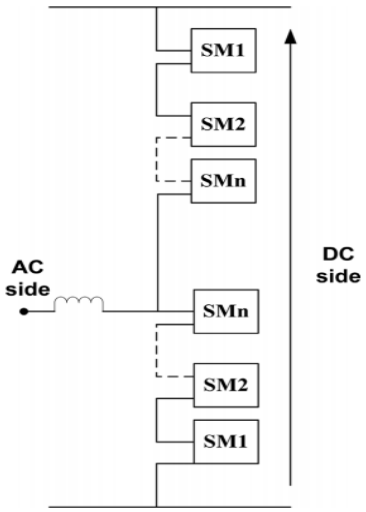

Figure 5. Architecture of a MMC multilevel converter.

A sub module is a half or a full bridge supplied by an electrical device. The higher or lower 1/2 a section is termed multilevel shown in Figure 5. The convertor arm acts sort of a versatile governable voltage supply since a sub module is controlled by selection or separately. Among the MMC features, we tend to mention a reduced fall, the use of non-Phase Shifted transformers with low insulation, high reliability attributable to the standard structure.

3.2. NPC derived structures

Various changed Nonproliferation Center topologies have conjointly been planned in the literature in recent years. as an example, new reduced topologies are developed in [11] therefore on achieve less cumbersome converters in terms of variety of elements and ride through the unequal losses distribution within the switches. In [12], the authors more devices exploitation IGBTs in parallel with the clamping diodes allowing this structure to own multiple management modes, Figure 6a. Parenthetically, it's potential to settle on the modulation type for equalization losses. a lively Nonproliferation Center topology (ANPC) was planned in [13]. By adopting a changed PWM strategy, this topology is in a position to double the apparent switching frequency and enhances the loss distribution balance in semi-conductors. Additionally, it permits the inverter to control underneath conditions of high and low switching frequencies.

A Stacked ANPC electrical converter was planned in [11] by adding in every arm, between the load and also the neutral point, a branch made from 2 switches nonparallel as shown in Figure 6b. Therefore, several redundancies making the intermediate level may be achieved that permits increasing the apparent shift frequency in comparison to the ANPC topology. This topology offers the advantage of using less shift devices with regard to the 2 previous structures. Though the likelihood of doubling the apparent shift frequency isn't any longer potential, redundancies will still be wont to portion losses within the different elements or maybe to limit the shift losses by attempting to reverse the fewest devices [14]. However, all the same Nonproliferation Center variants stay large and complex in terms of management. A shared Nonproliferation Center topology SASNPC was planned in [14].

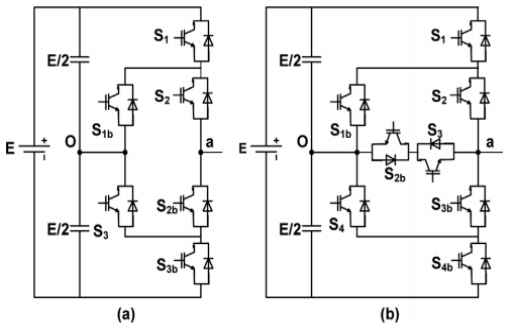

Figure 6. (a) Active NPC topology. (b) Stacked ANPC topology.

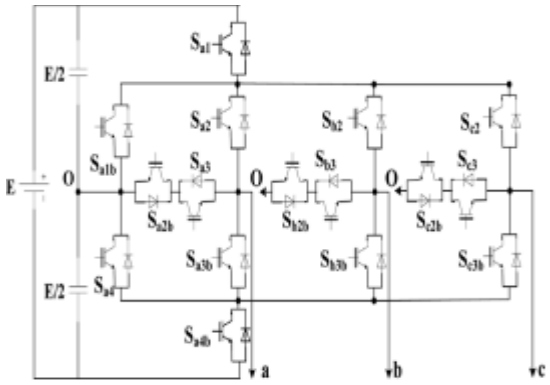

Figure 7. SASNPC topology.

Table 1. Active and passive components per phase for sevenlevel FC and PU Cells inverters.

Components	FC	PU Cells
Switches	12	6
Capacitors	6	2
Clamping Diodes	0	0

Table 1 provides the amount of active and passive elements (per phase) needed for basic FC, topology and element cells. As may be seen, the element cells topology has many advantages over the opposite ones. Compared to the seven level flying capacitors basic topology, the amount of capacitors is reduced from half dozen to two. Furthermore isolated DC sources do't seem to be obligatory.

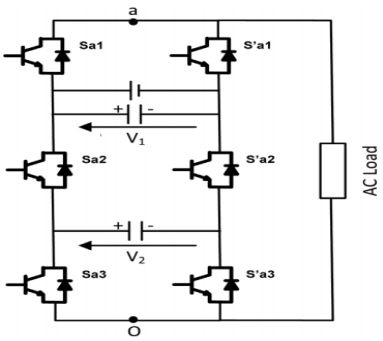

Figure 8. Seven-level Packed U-cells leg.

Its main feature remains, in the truth, that the 3 arms of the electrical converter share each upper and lower switches as delineated in Figure 7. As at any time 3 transistors ought to be turned on, so eight possible combos of the switch states may be synthesized? Among these combos, 2 zero redundant states (V0) and 6 active states (V1, V1-V2, V2, 0, -V2, V2-V1, and -V1) may be applied across the load.

3.3. FC Derived

A general power circuit of a seven level packed U cells converter (Only one phase) is pictured in Figure 8. Only two capacitors square measure needed for every leg. The primary one is used in parallel with the DC power supply (V1). Whereas the second permits, with the utilization of an impression circuit, the generation of a regulated voltage level (V2) that is necessary to supply the precise voltage levels across the load [15]. As is seen, solely six power switches square measure required for every leg. Every number of switches Sax(x=1, 2, 3) and S'ax square measure turned on in a very complementary manner.

4. Multilevel Inverters Hybrid Topologies

Generally, the cascaded H-bridge construction electrical converter is the basic topology subject to conjugation by merely exchanging a bridge by another of a unique sort. For the purpose of mastering the voltage capacitors unbalancing problems that seem with the 5L-NPC likewise like DC sources isolation of the H-Bridge, a compromise was established once developing a mixed topology shaped by 3L-NPC cells connected in cascade [48]. The ensuing topology referred to as cascaded 5L-NPC electrical converter produces therefore a 5 levels output voltage with a lot of compact structure and controlled DC voltage sources. In [49], the authors improved the output undulation quality that has been increased to nine by exploitation constant range of cells. Manjrekar et al. projected in [50] to mix 3 single-phase cells and a three-phase electrical converter office as depicted in Figure 9. This can cut back congestion as a result of the DC sources decrease from six to four, generating in addition a voltage of 9 levels.

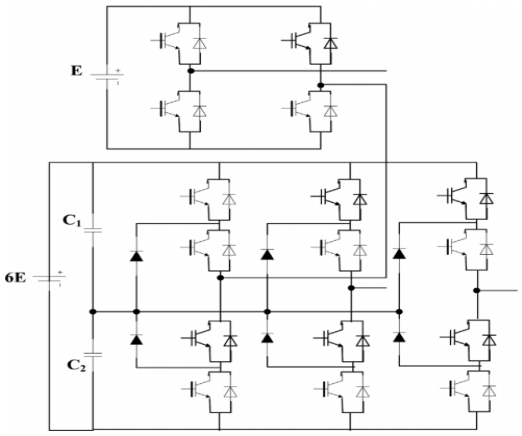

Figure 9. Hybrid multilevel inverter leg proposed by Manjrekar et al.

Another similar approach was given by Suh et al. [51]. The second H-bridge cell is substituted by a standard three-phase electrical converter. Just like the previous topology, this approach decreases the amount of elements principally the DC power sources compared to the electrical converter mentioned above. Contrary to any or all structures in cascades, the output voltage has a good range of levels. A symmetrical hybrid construction device with reduced number of insulated DC sources is projected in [52]. This topology may be a combination between the office and H-bridge inverter, Figure 10.

A full bridge is integrated to AN office main structure. The bridge's switches operate at low frequency switch. This structure is advantageous over the conventional cascaded construction electrical converter since it needs a reduced range of isolated DC sources.

Moreover, the switches range still constant. The 3 section configuration of this electrical converter has 2 common points, one to connect the electrical converter legs and also the alternative one is for load coupling. The road output voltage levels range is 2n+1 where n is that the DC supply range. It's obvious that the asymmetry within the DC voltage sources needs special care. The ability switches should face up to totally different rates of voltage stress. During this case, the utilization of devices happiness to distinct families is required. The IGCTs (Integrated

Gate-Commutated Thyristors) and HV-IGBTs (Insulate Gate Bipolar Transistors) area unit a lot of applicable for cells operating at high voltages [53], because of their massive voltage blocking capacities (over four.9 kV), their high efficiencies and their reduced losses [53]. As an example, LVIGBTs have sensible performances once operational at low frequencies [54]. Therefore, the idea of hybrid no longer considerations the idea of design however additionally includes the combination of semiconductors of various types within the same topology.

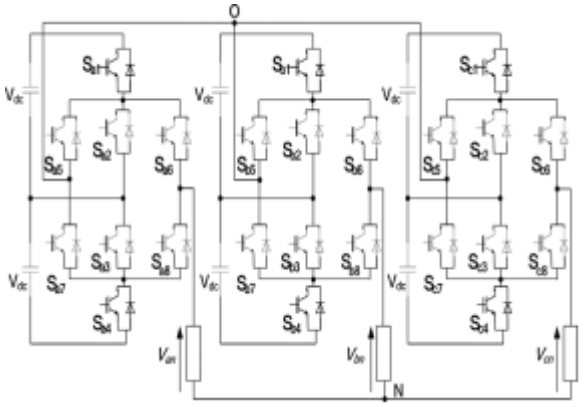

Figure 10. Symmetrical hybrid multilevel inverter with reduced DC supplies.

5. Voltage Quality Analysis

5.1. Voltage Harmonics Elimination

Modulation techniques square measure applied with the aim of controlling the inverter's output voltage and frequency as well on improve the standard of output waveforms. They are divided into 2 main classes [54]:

a. Operation at elementary change frequency: Selective Harmonic Elimination (SHE).
b. Operation at high change frequency: Pulse breadth Modulation (PWM) and area Vector Modulation (SVM).

5.2. Selective Harmonics Elimination

This methodology, as its name suggests, relies on the elimination of chosen harmonics typically dominant ones at low frequencies. The aim of SHE is so to scale back the total harmonic distortion of the output waveforms [55]. It consists in rotten the target output waveform into series. A system of transcendental equations reckoning on change angles (θ1..... θn) is thereafter established. The resolution of this method is done by conniving the opportune angles (θ1..... θn) using the Newton-Raphson methodology. The amount of calculated angles is up to the one amongst isolated sources within the case of the SHE at the elemental change frequency and it is totally different within the case of the SHE at high change frequency [48]. It ought to be underlined that this methodology could even be used at high change frequencies (SHEPWM). However, resolution of transcendental equations becomes additional advanced. The Newton-Raphson methodology is not economical as a result of it needs smart prediction of initial states. Recent algorithms were developed permitting additional accurate solutions by mean of Walsh functions [56] or neural networks [57].

5.3. Pulse Breadth Modulation

In this case, Modulation techniques square measure supported curved PWM with multiple carriers. This methodology consists in scrutiny a curved signal known as additionally modulating waveform with multiple triangular signals or carrier waves. The switches of every leg want (m-1) triangular signals having an equivalent frequency fp and therefore the same amplitude Ap. The reference sin waves square measure section shifted by 2π/3. Their amplitude and frequency square measure denoted Am and fm. The sinusoidal PWM technique is characterised by 2 ratios, the FM index megahertz = fp/fm and therefore the modulation ratio ma=Am/((m-1)Ap). Varied PWM modulation methods are rumored within the literature together with Phase Opposition Disposition (PO-PWM), Alternate section

Opposition Disposition (APOD-PWM), and section Disposition (PD-PWM) [58, 59]. All the said methods square measure supported PWM with multiple carriers however they disagree within the triangular signals disposition such as:

a. POD-PWM: the inner carriers around zero square measure 180° out of phase. Moreover, every few triangular signals above and below zero is in section.
b. APOD-PWM: each 2 resulting carriers square measure section shifted by 180°.
c. PD-PWM: all the carriers square measure in section.

5.4. Selective Harmonics Elimination

The area Vector Modulation (SVM) technique uses a space vector that represents the 3 reference output voltage waveforms. Hence, an area vector modulation algorithm ought to verify at every sampling time the appropriate change states that best approximate the reference vector. Generally this vector is synthesized by using a combination of the closest 2 active voltage vectors and a zero vector [60-64].

The SVM is convenient for digital implementation on digital signal processors and permits top quality output waveforms with improved harmonic content. The implementation of a SVM involves 3 steps.

• Identification of the Triangle within which the tip purpose of the reference vector is lying.

• Calculation of duty cycles for every triangle.

• Identification of shift states in keeping with a desired switching sequence. In general, the approaches planned in the literature take issue chiefly within the manner of locating the reference vector. Among the few analysis works planned in literature, we discover in [61] a remarkable approach that allows the direct identification of the adequate triangle whereby the tip purpose of the reference voltage vector falls. In [62] the authors begin from the very fact that the space-vector diagram of a three-level electrical converter is composed of six tiny hexagons that area unit the space vector diagrams of two-level inverters. These small hexagons are known by dividing the area vector diagram into six sectors as shown in Figure 9.

At any sampling time the reference voltage vector is located at intervals these six small-hexagons, then a brand new reference voltage vector should be outlined. During this manner, the three-level space-vector is simplified to a two-level space vector. It ought to be noted that once the amount of levels increases, the employment of this algorithmic program becomes tedious. Another approach applied to three-level inverters has been planned in [63] wherever the area vector diagram of a three-level inverter was transformed from (α, β) frame to a polygonal shape reference system (h, g). It follows that each one switching vectors have whole number coordinates. The reference voltage vector is thenceforth set at intervals AN equal-sided parallelogram that makes straightforward the identification of the three nearest vectors. Another area vector approach was planned in [60], wherever AN m-level reference voltage vector has been created from the lower level reference vector.

In [60], the authors thought of that the area vector diagram of AN m-Level electrical converter features a shape structure, where the fundamental structure may be a triangle. Every sector was considered as an outsized triangle. By victimization shape theory, each triangle was divided into four tiny triangles. The authors planned therefore a triangularization algorithmic program for identifying the acceptable triangle that encloses the tip point of the reference voltage vector. It ought to be noted that the amount of iterations of triangularization algorithmic program becomes a lot of higher because the variety of levels will increase.

5.5. Voltage Quality Bounds

According to the out there literature, the sole works defining and quantifying the ThD bounds of construction inverters output voltages area unit those of Ruderman in [41- 44]. The author argues that several recent construction electrical converter papers find you with voltage ThD analysis results that are generally supported voltage frequency spectra numerical calculations/measurements (FFT). A possible issue could be a limited variety of accounted harmonics. as an example, accounting for forty nine harmonics (as suggested by IEEE Standard 519) could deliver basically underestimated voltage THD. Numerically calculated line (line-to-line) and phase (line-to-neutral) voltage ThD for a three-phase balanced load with isolated neutral could become completely different. However, tho' line and part voltage spectra area unit completely different (triplen harmonics don't seem within the line voltages), line and part voltage ThD during this case area unit basically the same that's nearly evident from a time domain thought [42]. Given numerically calculated or measured voltage ThD, it's going to be troublesome to evaluate concerning voltage quality whether or not it's adequate or bad? Will the voltage THD be subjected to the calculation or measure errors? So, it's instructive to elaborate theoretical bounds for best nearest switch voltage quality.

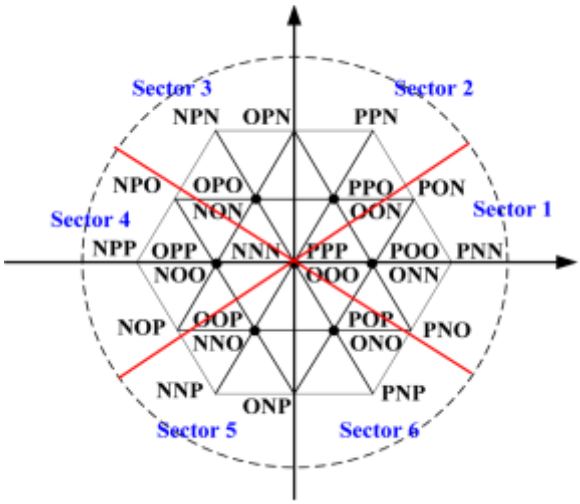

Figure 11. (Color online) Small hexagons constituting the space vector diagram.

As mentioned antecedently, voltage quality for single and three-phase construction inverters with high switch frequencies was thought of in [41-44]. The belief of infinitely giant switch frequency has junction rectifier to A higher bound of voltage quality for synchronous nearest switch. In distinction, the lower voltage quality certain was achieved for a borderline quantity of synchronous switch between any 2 adjacent voltage levels. The author approximated swish ThD higher and lower bounds by (11) and (12).

$$\mathrm{THD}_{\mathrm{up}}(\mathrm{L},\mathrm{M}) = \frac{57.7}{(\mathrm{L}-1)\mathrm{M}}\ \% \tag{11}$$

$$\mathrm{THD}_{\mathrm{low}}(\mathrm{L},\mathrm{M}) = \frac{47}{(\mathrm{L}-1)\mathrm{M}}\ \% \tag{12}$$

Figure 12 exhibits associate example of higher and lower bounds hyperbolic curves as perform of modulation index for three and five Levels.

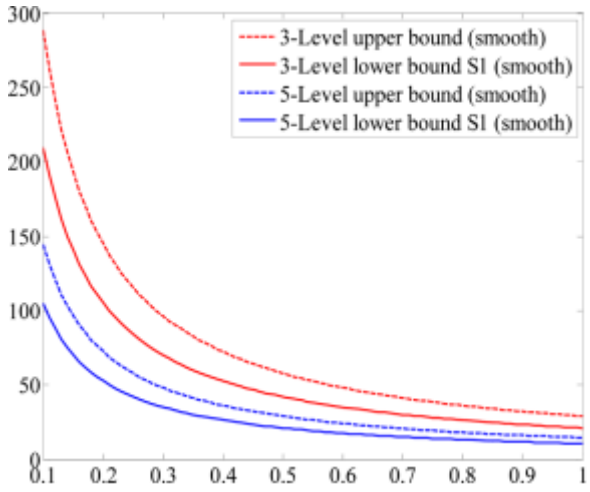

Figure 12. (Color online) Smooth upper and lower bounds for three and five levels.

Although the current paper could be a review, many numerical simulations with the most topologies (CHB, NPC, FC) were administered during this section so as to verify the Ruderman formulas. Simulations parameters are:

1. Frequency ratio: mc = 100
2. Sinusoidal wave: fp = 50 Hz
3. Carrier: fm = 5 KHz.

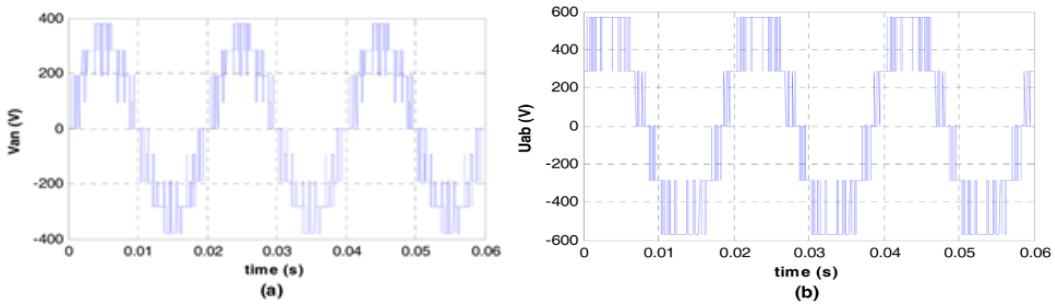

Figure 13. (Color online) Five level CHB converter output voltage waveforms: (a) Phase voltage Van and (b) line voltage Uab.

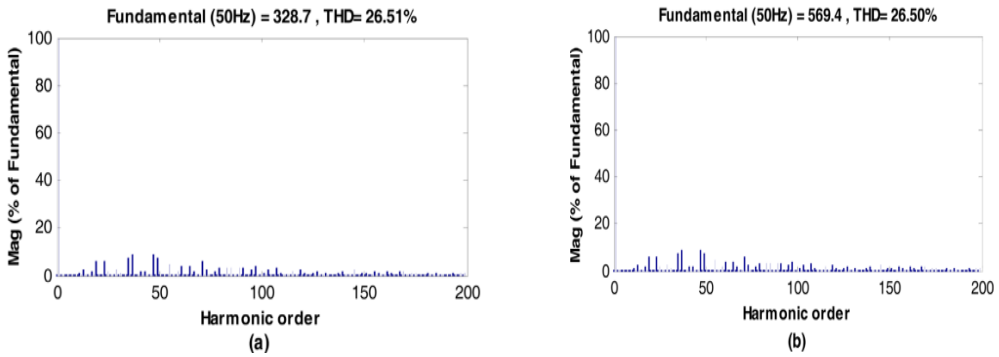

Figure 14. (Color online) (a) Phase and (b) line harmonic spectrums of five level H-bridge.

After playacting the required simulations, it had been shown that the everyday waves of the FC, federal agency and H-bridge multilevel inverters (isolated neutral) area unit virtually a similar. To avoid repetition and area intense, solely output voltage waveforms similarly as their harmonic spectrums relative to the CHB topology area unit according in Figure 13 and 14 just in case of five levels. Instead, all simulation results area unit resumed in Table 2 and Table 3.

Table 2. THD of line and phase voltages for five level CHB, NPC and FC inverters, M = 1.

Type of MLI	Van THD%	Uab THD%
CHB	26.51%	26.50%
NPC	26.91%	26.92%
FC	26.95%	26.96%

Table 3. Voltage quality bounds for five, seven and nine level H-Bridge inverters, M = 1.

THD	5-Levels	7-Levels	9-Levels
THDup	28.85%	19.23%	14.42%
THDlow	23.5%	15.66%	11.75%
THDcalculated	26.5%	18.38%	13.55%

Even if it's obvious that, the load section voltage Van has a number of levels considerably on top of Uab, Figure 13, and the calculated THDs of line and section voltages area unit quite similar regardless of the construction device is, Table 2. Referring to (14) and (15), the higher and lower bounds are calculated for 5L and 9L H-bridge converters wherever an m cascaded construction device operational below a modulation index M up to one offers a line to line voltage with L = (m-1)/2 non negative levels [41]. Indeed, the estimated Doctor of Theology values area unit among the interval [THDup, THDlow] as illustrated by Table 3, proving the truthfulness of the Ruderman formulas a minimum of for M = one.

6. Conclusion

This paper has reviewed the state of the art of structure inverters. Varied structure topologies are reviewed together with major structures additionally as their derived and hybrid ones. Despite the wide selection of recent multilevel configurations, they continue to be on the shadow of the basic topologies that are office, H-Bridge and FC. This work conjointly investigated easy modulation paradigms. The most relevant techniques for harmonic elimination, in order to boost the output voltage quality, are cited. The presented ThD voltage formulas, given within the literature, are also reportable and verified by acceptable simulations for some modulation indexes. It's to be stressed that the choice of the convenient electrical converter kind may be a exchange which clearly depends on the applying and therefore the desired achievements.

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