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Design Analysis and Development of Inverter Topologies for Industries

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ABSTRACT

This paper presents the most common inverter topologies and its design, analysis and development schemes. The main objective is to design and compare the three topologies of multilevel inverter for industries. These three topologies are mostly effectively and efficiently for quality improvement of the output voltage waveform of inverter. Photovoltaic (PV) and wind power generation (WPG) i.e. the renewable energy systems are playing a vital role in energy production. But, solar photovoltaic power (PV) has the prospective to develop one of the foremost suppliers to the future electricity supply. Therefore, Low voltage solar PV systems need a high voltage expansion converter for units of grid connection with multilevel inverter. The multilevel inverter topologies are being used in applications of medium and high power such as an active power filter, FACTS devices and a machine current due to their various merits in terms of power supplies low power dissipation, low harmonic distortion in voltage output waveform. Therefore, the simulation of multilevel inverter topologies is done and finalized that cascade multilevel inverter topology is more suitable as compared to other two by using MATLAB/SIMULINK.

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1. INTRODUCTION

In modern years, many applications of industries have initiated to require medium or high power for their task [1]. But, it is very difficult for a grid medium voltage to associate directly a single power rating of semiconductor switch. A multilevel power inverter arrangement has been presented since 1975 for example an alternative in high power and medium voltage situations and the arrangement of switching angles are very important. Multilevel inverter goes up to high switching voltage using a sequence of step voltages, each of which is depend on the power devices rating individually. For multilevel inverter, some topologies are classified in two groups depending on the number of independent dc source. In recent years, the greatest corporate topologies are diode-clamped/neutral-point inverter (NPC), flying capacitor/capacitor-clamped (FC) inverter and cascade H-bridge (CHB) inverter. The topology of NPC is some way similar to the FC with difference that flying capacitors are replaced by clamping diodes. CHBs inverters are classified by series connection of two or more single-phase H-bridge inverters. Fundamental switching frequency and high switching frequency PWM methods are used to operate the multilevel inverters by means of efficiency high and switching losses low. In the CHB multilevel inverter (MLI), a separate DC voltage source is required for each level and a PV cell or battery is to be connected for each DC source.

2. DIODE CLAMPED MULTILEVEL INVERTER

A 3-level diode-clamped inverter correspondingly so-called the neutral clamped inverter presented by Nabae, Takahashi and Akagi popular 1981 [1]. Some research scholars published articles that have conveyed outcomes up to 4, 5 and 6-level diode clamped inverters. After reading [1]-[5], we conclude that for a 1-Φ three-level neutral clamped inverter at any given time a set of 2 switches is ON. This type of inverter is suitable on an AC transmission line for transmission of DC current or variable speed motors.

In Figure 1, the output voltage in DC is separated in series form of two bulk capacitors C_1 and C_2 into 3 levels. The two diodes D_1 and D_1' hold the switch voltage to the DC-bus voltage of half level. And, when we turn ON the switches S_1 and S_2, the the terminals voltage across a and 0 is V_{dc}, i.e., $V_{ao}= V_{dc}$. Note the output voltage Vao is DC and Van is AC. The voltage difference between voltage V_{an} and V_{ao} is the voltage across the capacitor C_2, which is $V_{dc}/2$ as in Table 1.

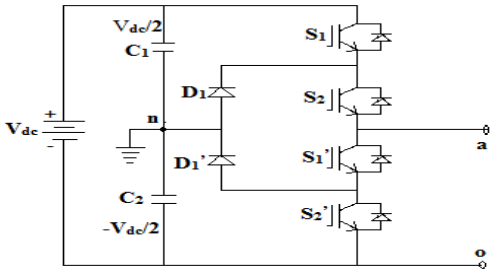

Figure 1: Three level diode-clamped inverter

Table 1: Switching Pattern for 3-level Diode-clamped Inverters

Sequence of Switches (ON)	Load Voltage
S1, S2	+Vdc/2
S1', S2'	-Vdc/2
S2, S1' or S1, S2'	Zero

In Figure 2, a 3-Φ 7-level diode-clamped inverter is given and a common voltage DC bus is joint by each of the 3- Φ which is subdivided by 6 capacitors into 7-level [6].

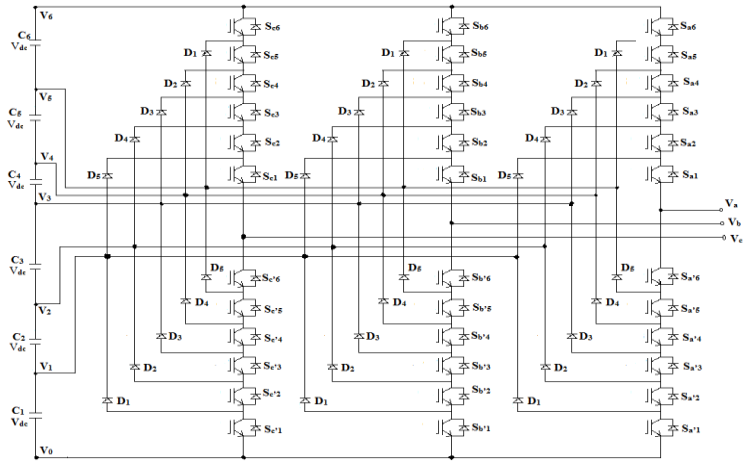

Figure 2: 3-Φ, Seven-level diode-clamped inverter

The output possible voltage levels for each inverter phase with reference to zero i.e. voltage V_0 is shown in table 2 [6]. When the switch of semiconductor device is ON, the state condition is one (1) and when the switch of semiconductor device is OFF, the state condition is zero (0). It has 6 corresponding switch pairs in each phase so that turning ON one of the switches of the pair require that its other corresponding switch is to be turned off. The corresponding switch pairs for phase leg 'a' are (S_{a1}, $S_{a'1}$), (S_{a2}, $S_{a'2}$), (S_{a3}, $S_{a'3}$), (S_{a4}, $S_{a'4}$), (S_{a5}, $S_{a'5}$) and (S_{a6}, $S_{a'6}$). The line voltages V_{ab}, V_{bc} and V_{ca} involves of a phase a-b, b-c and c-a voltages respectively. When the lower switches all $S_{a'1}$ through $S_{a'6}$ are turned ON, D_5 must block 5 voltage levels or $5V_{dc}$ as per table 2 for phase 'a'. Similarly, D_4 must block $4V_{dc}$, D_3 must block $3V_{dc}$, D_2 must block $2V_{dc}$ and D_1 must block V_{dc}. If we designed this inverter, each blocking diode has the same voltage rating; D_n will need 'n' diodes in series.

Table 2: Voltage Levels and Equivalent Switch States for 7-level, 3-Φ Diode-Clamped Inverter

Voltage Vao	**Switch State**											
	S_{a6}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'6}$	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_6 = 6*V_{dc}$	1	1	1	1	1	1	0	0	0	0	0	0
$V_5 = 5*V_{dc}$	0	1	1	1	1	1	1	0	0	0	0	0
$V_4 = 4*V_{dc}$	0	0	1	1	1	1	1	1	0	0	0	0
$V_3 = 3*V_{dc}$	0	0	0	1	1	1	1	1	1	0	0	0
$V_2 = 2*V_{dc}$	0	0	0	0	1	1	1	1	1	1	0	0
$V_1 = V_{dc}$	0	0	0	0	0	1	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	0	1	1	1	1	1	1

3. FLYING CAPACITORS MULTILEVEL INVERTER

In 1992, Meynard and Foch presented a flying capacitor (capacitor clamped) typed inverter [1]. This inverter circuit is just like a diode-clamped inverter. The design needs single 2 switch combinations to generate an output voltage waveform.

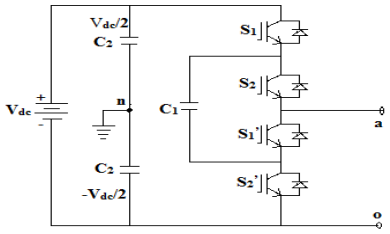

Figure 3. 3-level type capacitor–clamped inverter

The inverter offers a 3-level output voltage waveform across terminals a and n, i.e., $V_{an}= V_{dc}/2$, 0, or $–V_{dc}/2$ as shown in figure 3. For voltage level $V_{dc}/2$, switches S_1 and S2 requisite to be turned ON; for voltage level $–V_{dc}/2$, switches S_1' and S_2' requisite to be turned ON; and for voltage level 0, either pair (S_1,$S_{1'}$) or (S_2,$S_{2'}$) desires to be turned ON. In figure 4, a 3-Φ 7-level capacitor-clamped inverter is given (similar of figure 2) [6].

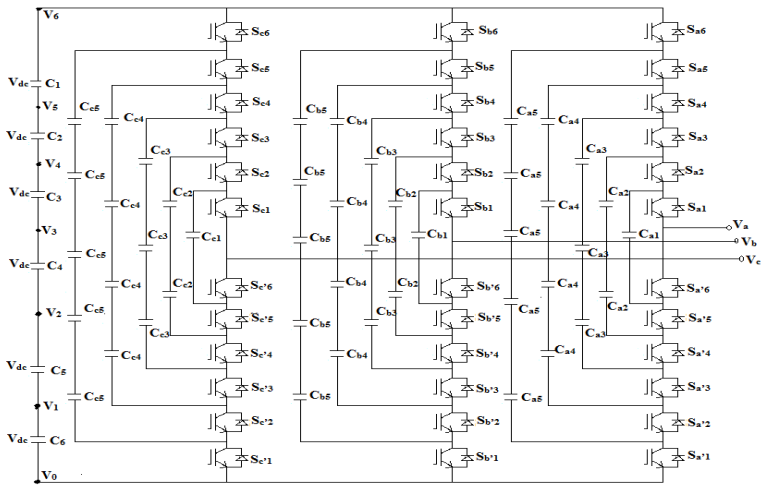

Figure 4. 3-ϕ, 7-level capacitor–clamped inverter

4. CASCADED H-BRIDGE MULTILEVEL INVERTER

In 1995, Manjrekar introduced a cascade H-bridge typed inverter [1]. In this paper, a cascade multilevel inverter in each phase requires ‘s’ DC sources for (2s+1) level. For the interest purpose we can use e. g. battery, fuel cell of a DC power source [7]. A 3-Φ building block of a 13-level cascade multilevel

inverter (CMI) using 6 SDCSs is designed as shown in figure 5 as per the table 3 configuration for each H-bridge inverter. The topology of multilevel inverter has the minimum components as compared to other topologies for a specified number of levels.

Table 3: Switching Pattern for H-bridge Inverters

Sequence of Switches (ON)	Load Voltage (V_{co})
S_1, S_4	$+V_{dc}$
S_2, S_3	$-V_{dc}$
S_1, S_4 or S_2, S_3	Zero

The Cascaded 13-level inverter necessitates 6 separate DC sources per phase leg; this means that 6, H-bridge inverters are used for 1-Φ structure. Each 1-Φ, 13-levels CMI is connected as star it means that one of the terminals is connected at common point and the other terminal is connected to a 3-Φ series load [7].

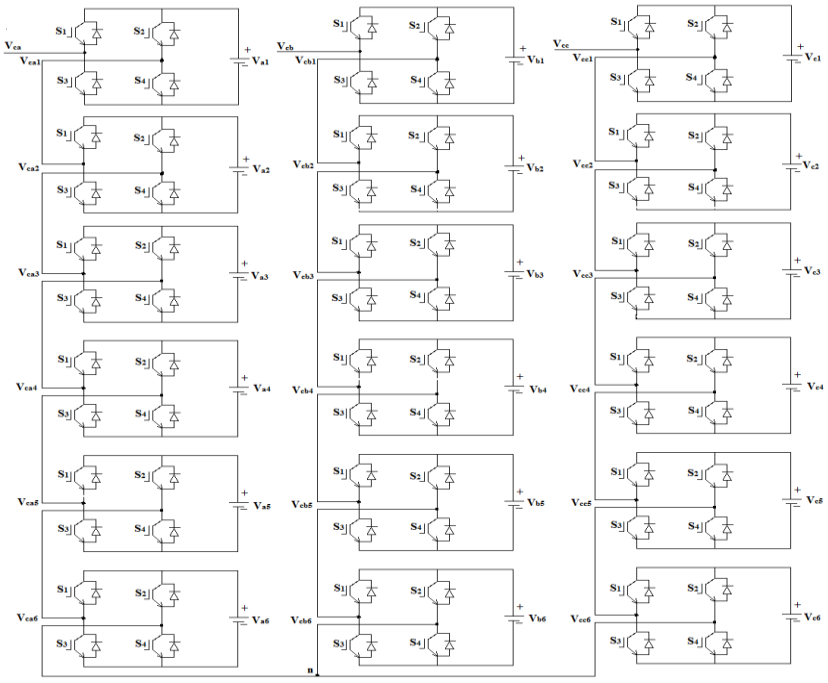

Figure 5. 3-Φ, 13-level cascaded h-bridge inverter

The output phase voltage is synthesized by the addition of outputs of individual inverter, for example, the phase voltage of 'a' in 13-level is:

$$V_{ca} = V_{ca1} + V_{ca2} + V_{ca3} + V_{ca4} + V_{ca5} + V_{ca6} \quad (1)$$

5. COMPARISON OF DIFFERENT TOPOLOGIES IN MULTILEVEL INVERTER

As compare to other two, cascade multilevel circuitry is simple because it doesn't have extra auxiliary capacitors and diodes. And, we can be found the level of the voltage on each stage, number of output level and number of switches values by formulas which is used in these topologies as shown in table 4. There are many types of modulation control methods that we have used to control it i.e. selective harmonic elimination or harmonic optimization (SHEM), space vector PWM, sinusoidal pulse width modulation (SPWM) and active harmonic elimination. But, SHEM technique is simple, show less harmonic and efficient output voltage waveform and it completely depends on the no. of levels information. The selective harmonic elimination method is more appropriate for a multilevel inverter circuit and low Total Harmonic Distortion (THD) output voltage waveform is possible without any filter circuit for using this technique.

$$V_n = \frac{4V_{dc}}{\pi}\sum_{n}^{\infty}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\frac{\sin(nwt)}{n} \quad (2)$$

Where :
Vn = amplitude of voltage harmonic of nth order,
Vdc = DC voltage
s = number of the bridges in each phase
n = odd harmonic order

$$H(n) = \frac{4}{\pi n}\sum_{n=1}^{\infty}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \quad (3)$$

Table 4: Comparison of Topologies in Multilevel Inverter and Corresponding Equipment which are used in Circuit

S. No.	Name of the Topology	Level of the Voltage on each Stage	Number of Output level (m)	Number of Switches used	No. of diodes	No. of DC link Capacitors	No. of Auxiliary Capacitors
1.	Diode Clamped Multilevel Inverter	VS on each DC link capacitor 'C'	{Number of Capacitors+1}	2(m-1)*n Where, n=no. of phases	(m-1)*(m-2)	m-1	Zero
2.	Flying Capacitors Multilevel Inverter	VS on each DC link capacitor 'C'	{Number of Capacitors+1}	2(m-1)*n	Zero	m-1	n*(m-1)*(m-2)/2
3.	Cascade H-bridge Multilevel Inverter	sVdc Where, s=no. of sources	2s+1	4s*n or 2(m-1) *n	Zero	Zero	Zero

6. EXPERIMENTAL WORK

The figure 6 and 9 give the voltage difference between voltage V_{an} (AC output) and V_{ao} (DC output) is the voltage across the capacitor C_2, which is $V_{dc}/2$ (V_{dc} =100V) as shown in figure 7, 8 and figure 10, 11 respectively. But in figure 12 with fewer components as compared to other two topologies, output AC voltage is V_{dc} as shown in figure 13.

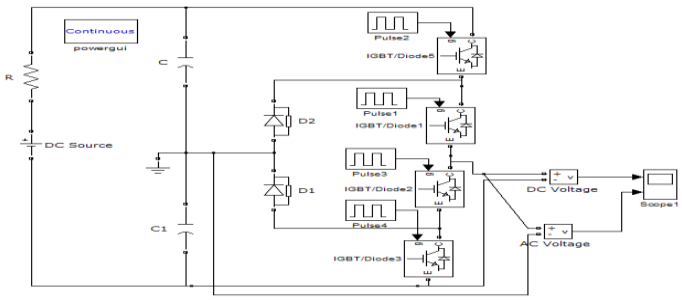

Figure 6: Simulated circuit diagram for 1-ϕ, diode-clamped inverter

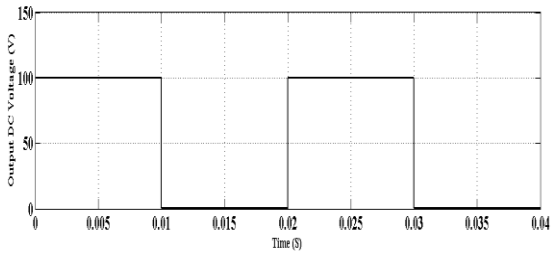

Figure 7: 1-Φ, Output DC voltage of diode-clamped inverter

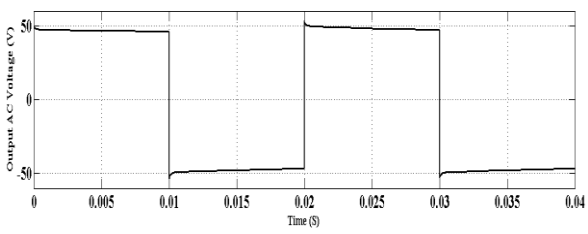

Figure 8: 1-Φ, Output AC voltage of diode-clamped inverter

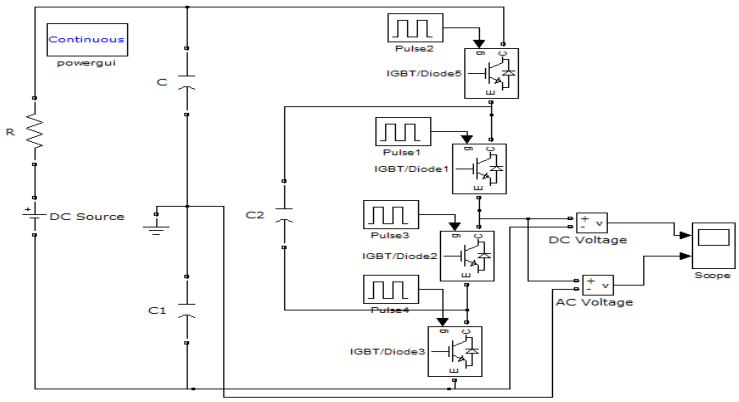

Figure 9: Simulated circuit diagram for 1-ϕ, capacitor-clamped inverter

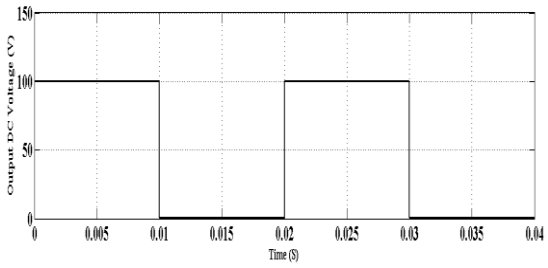

Figure 10: 1-Φ, Output DC voltage of capacitor-clamped inverter

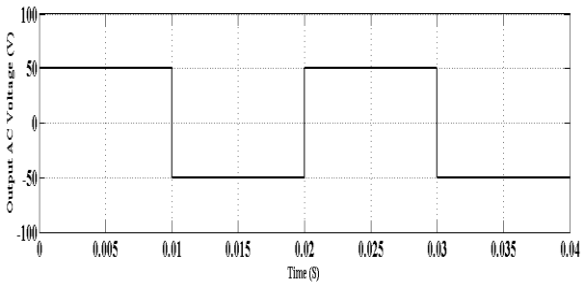

Figure 11: 1-Φ, Output AC voltage of capacitor-clamped inverter

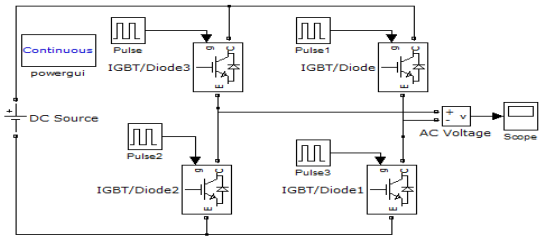

Figure 12: Simulated circuit diagram for 1-ϕ, h-bridge inverter

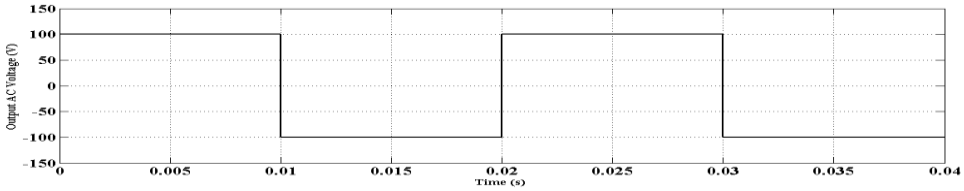

Figure 13: 1-Φ, Output AC voltage of h-bridge inverter

The simulated circuit diagrams for 1- Φ and 3- Φ cascade 13-level inverter are presented in figure 14, 17 and simulated output voltage, current waveforms i.e. 1- Φ, 3- Φ are shown in figure 15, 18 and 19 respectively. Additionally, Figure 16 shown the FFT signal for the line-to-line output voltages of the 13-level CHB and the THD is found to be 15.27%.

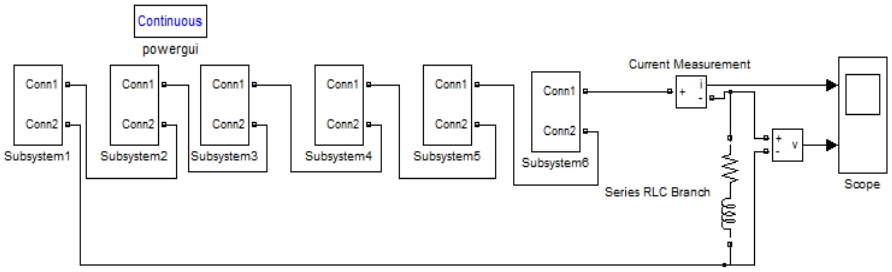

Figure 14: Simulated circuit diagram for 1- ϕ, cascaded 13-level inverter

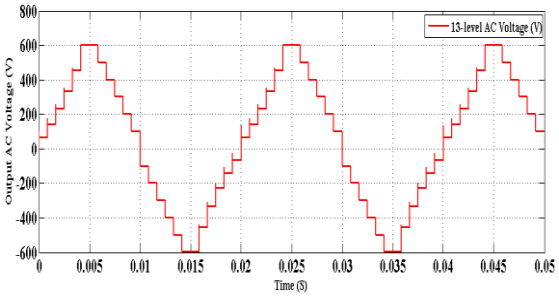

Figure 15: 1-Φ, Output AC voltage waveform of cascaded 13-level inverter

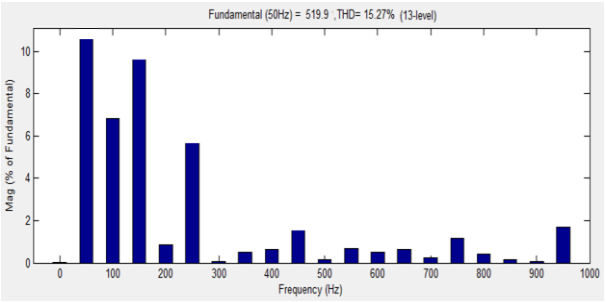

Figure 16: FFT analysis of 13-level CMI (Total Harmonic Distortion=15.27%)

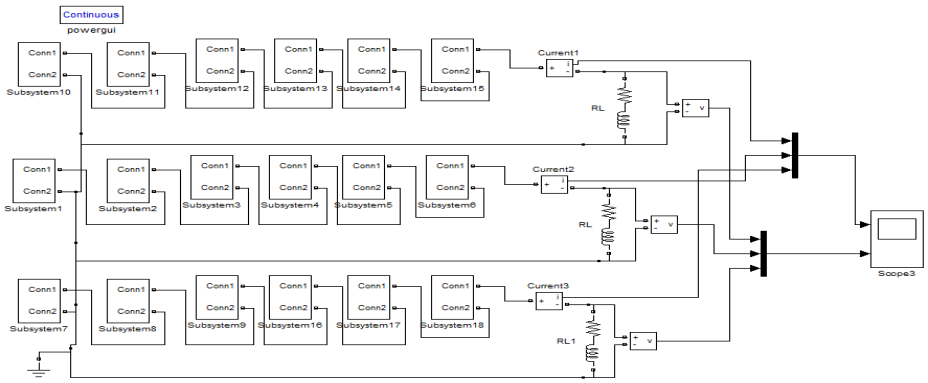

Figure 17: Simulated circuit diagram of 3-ϕ circuit of cascaded 13-level inverter

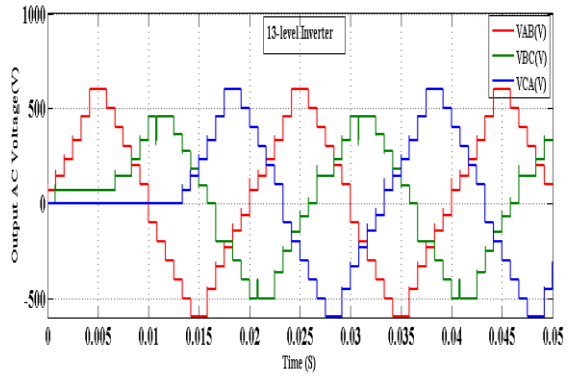

Figure 18: 3-Φ, output AC voltage waveform of cascaded 13-level inverter

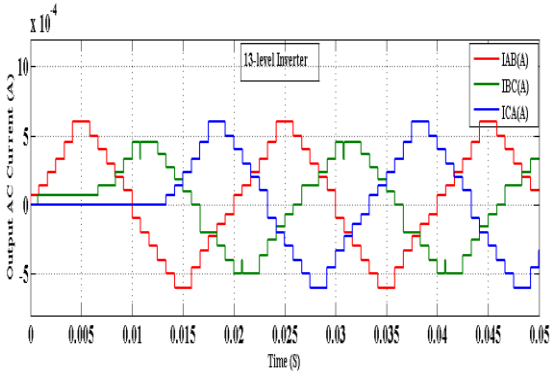

Figure 19: 3-Φ, output ac current waveform of cascaded 13-level inverter

Analyzing these results indicates that the cascade structure has less total number of elements comparable to the other topologies. Instead, it displayed a higher number of power sources, which can be taken as an advantage leading to limit the stress on the switches and decrease the THD.

7. CONCLUSION

The ceremonial of the art of multilevel power inverter technology for different three topologies is demonstrated in this paper. Therefore, after designing these topologies we established that cascade H-Bridge inverter is superior to others while we compare the modulation structure, reliability and switching methods with other two topologies. For manipulative the required output voltage level on each step in each topology, a procedure has been clearly defined and the required number of switches also increased as the number of levels in the conventional methods is increased. Finally, Matlab/Simulink based model for 3-level of these three topologies and cascaded 13-level inverter is developed and simulation results are presented.

REFERENCES

[1] Jih-Sheng Lai and Fang Zheng Peng, Member IEEE, "*Multilevel Converters-A New Breed of Power Converters*", *IEEE Transaction on Industry Applications*, May/June 1996, 32(3).

[2] Wanki Min, Joonki Min and Jaeho Choi, "*Control of STATCOM using Cascade Multilevel Inverter for High Power Application*", *IEEE International Conference on Power Electronics and Drive Systems*, Hong Kong, July 1999.

[3] Jose Rodriguez, Jih-Sheng Lai andFang Zheng Peng, "*Multilevel Inverters: A Survey of Topologies, Controls, and Applications*", *IEEE Transactions on Industrial Electronics*, August 2002, 49(4).

[4] F. Z. Peng, J.W.McKeever and D.J.Adams, "*Cascade Multilevel Inverters for Utility Applications*", *IEEE Transactions on Power Electronics*, February 2003, 17(6).

[5] Chang Qian, Mariesa L. Crow, "*A Cascaded Converter-Based STATCOM with Energy Storage*", *IEEE* 2002.

[6] Sunita Kumari and Sudhir Y Kumar, "*Design And Control of Multilevel Inverter Topologies for Industrial Applications*", *International Journal of Mechanical Engineering and Technology (IJMET)*, June 2017, 8(6):107-116.

[7] Dnyaneshwar D. Khairnar, V. M. Deshmukh, "*Review Study on Topologies of Multilevel Inverters*", *IJIRD* ISSN: 2278-0211, May 2014, 3(5).

[8] Sunita Kumari, Sudhir Y Kumar, "*Design of Cascaded Multilevel Inverter for Harmonic Distortion Elimination*", *IJEETE*, Mar-Apr 2017, 04(02):102-108.

[9] J. Yuncong, J. A. A. Qahouq, and M. Orabi, "*Matlab/Pspice hybrid simulation modeling of solar PV cell/module*", *Applied Power Electronics Conference and Exposition (APEC), Twenty-Sixth Annual IEEE*, 2011:1244-1250.

[10] Chatterjee, A. Keyhani, and D. Kapoor, "*Identification of Photovoltaic Source Models*", Energy Conversion, *IEEE Transactions*, 2011:1-7.

[11] Miska Prasad, Ashok Kumar Akella, "*Performance Evaluation of Three Different Inverter Configurations of DVR for Mitigation of Voltage Events", Indonesian Journal of Electrical Engineering and Informatics (IJEEI)*, December 2016, 4(4): 225-239.

[12] S. Daher, et al., *"Multilevel Inverter Topologies for Stand-Alone PV Systems", Transactions on Industrial Electronics*, 2008, 55(7): 2703-2712.

[13] Yogita Kumari, Anmol Gupta, Shiv Prakash Bihari, R. N. Chaubey and B. Sehgal, "*Performance and Analysis of Reactive Power Compensation by UPFC", Indonesian Journal of Electrical Engineering and Informatics (IJEEI)*, September 2015, 3(3): 141-149.

[14] S. Dasam and B. V. Sankerram, *"Voltage Balancing Control Strategy in Converter System for Three-Level Inverters", International Journal of Electrical and Computer Engineering (IJECE)*, 2013, 3(1): 7-14.

[15] M. Satyanarayana, P. Satish Kumar, "Analysis and Design of Solar Photo Voltaic Grid Connected Inverter", *Indonesian Journal of Electrical Engineering and Informatics (IJEEI)*, December 2015, 3(4): 199-208.