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PV Systems based High Gain Converter using CI and SCC Techniques

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ABSTRACT

In this paper, new techniques for a CI (coupled inductor) and SCC (Switched Clamp Capacitor)-based stepup higher-level voltage DC-DC converter were implemented. The CI and SC, charge and discharge the energy, respectively, to attain higher gains. Using the clamp circuitry, the stress on the switching volt level and inductance leakage are removed. The reversed retrieval problem in the diode was eradicated with the help of a coupled inductor (CI). The new topology is to get more gain from the voltage and improve efficacy. The steadystateexamination of novel DC-DC converteroperation procedures arediscoursed here. The proposed model has an inputvoltage of 24V and an outputvoltage of 410V. Pmax of 150Wwas given to get a maximum of 96.4%.

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1. INTRODUCTION

Our country is deeply concerned about the energy crisis and environmental issues [1]. In this concern, the global warming problem will occur, and this will in turn increase the level of the sea by about 2 meters. This has a greater impact on the lives of all human beings. Non-conventional energy sources are used to resolve the air pollution and energy crises and global warming problems. Non-conventional Energy causes like sun_energy, energy from the wind, and wave_energyis widely used. [2], [3], [4]. Non-conventional energy sources produce a lower voltage level and it must be increased by using a converter named stepper-up boost DC-DC. This higher voltage output is transferred through the inverter to convert DC into AC [5] [6] [7] [8]. The stepper-up boost DCDC converter ratio disturbs entire system efficacy. The existing convertercircuit topology is not suitable for Steper-Up Boost dc-to-dc converter ratio applications. In existing Stepper-Up Boost dc-to-dc converter circuit, the duty cycle is increased to 1. During ideal conditions, the Stepper-Up boosting conversion ratio should reach its maximum value. The Stepper-Up Boost DC-DC Converter circuits EMI and Converse retrieval problems are issued to limit the high voltage gain by using the C, L, R, and switches. The leakage of the transformer affects the huge amount of power dissipation and a large amount of voltage spike problems occur on switch.

Selection of power switches with highvoltage stress is the main consideration because of redundant cost and more space problems. To introduce the new architecture, the existing method of the boost converter circuit problems is overcomed. The new architecture of the switched capacitor [9], [10], [11], [12], [13] coupled inductor [14 to 21], and lifting of voltage techniques [22] [23] are proposed. The minimum amount of energy strain in switching circuits with an upsurge in alteration ratio of voltage is achieved by using an inductive structure of a coupled inductance stepper-up boosting converter circuit. This type of technique is mostly used,

but the main disadvantage of these techniques is the leakage inductance of the CI and spikes in voltage. The snubber circuit is used to solve issues like leakage inductance and spikes in voltage. A higher stepper-up boosting ratio function is attained by using techniques of a switchedcapacitor and boost of voltage techniques, but more transient current and conduction losses occur on the chief switch. In this case, switch 'S' will be turned on, and in turn, a switch-based capacitor will be utilised to back up the energy. When power volt is zero, energy stored in capacitor-unit is utilisedfor discharging energy back to the load-unit. Lift of voltage techniques are similar to a SEPIC converter or a CUK converter in terms of energy transfer from L-C-L. This energy transfer from the inductor to the capacitor affects the current stress on the capacitor. [24] [25]. The boost stepper-up flyback converter-based switch capacitor techniques produce a huge amount of step-up ratio. In this technique, the switch is ON condition that the boost converter starting stage is the same as the amalgamation of the booster-based converter with SC. The turned-off mode of the switch represents the 2nd stage of the boost converter, and the same is similar to the combination of fly back with an SCC [26 to 37]. The proposed method of adjusting the duty cycle can reach a maximum boost. By using the clamp circuit to produce high efficiency, we can minimise the leakage inductance of the energy recovery from the CI (coupled inductor). A large voltagegain can be achieved without operating at extreme duty cycles, that is ideal for renewables. A single current switch is simple to operate for the appropriate output volts, generality capability is required. A passively voltage clamping circuit that reduces overvoltage on the switch, recovers inductance leakage energy, and boosts a converter's voltage output. It will resolve the issue of diode reversal restoration. The switching loss was reduced by using fewer voltage-stress components and a minimum conducting resistance R_{ds} and to get a maximum efficiency of almost 96.4%.

2. HIGH GAIN CONVERTER CONVERTER

The new high gain converter circuit consists of the input voltage of a DC supply, the primary switch S, coupled inductors N_p and N_s as represented below in Figure 1. V_1 and V_2 are the RMS voltages at the input and output of RC correspondingly.

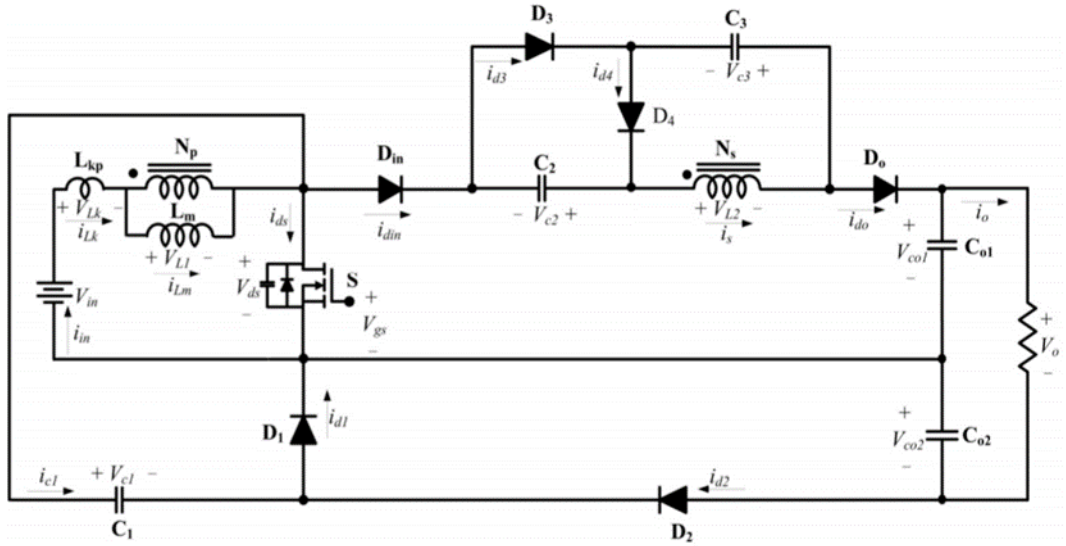

Figure 1. Planned Converter Circuitry

Clamp circuit consists of the diodes D_1, D_2 and C_1. The Stepper-Up boost-circuitry consists of D_3andD_4 diodes, capacitors of C_2andC_3. The coupled inductor equal circuits consist of L_k (leakageinductor) and L_m (magnetizing inductor) and the primary and secondary windings turns N_p and N_s of the ideal transformer. The proposed converter operating principle and the below conditions are considered

- C_1, C_2, and C_3 capacitors, as well as C_{01} and C_{02}, are adequately large.
- Capacitor voltages V_{c1}, V_{c2}, and V_{c3}, assumed to be constant.
- Consider power devices as ideal components, with parasitic capacitors neglected.
- The coupling inductor K's co-efficient is the same as $L_m*/(L_m*+L_k*)$.
- n (ratio of turns) = N_s*/N_p*

The two-mode operator procedures of the projected converter

- Continuous Conduction Mode
- Discontinuous Conduction Mode

A. Continuous Conduction Mode

Continuous Conduction Mode of operation's voltage and power waveform is represented in Figure 2. Five operating modes of continuous-conduction are:

I Mode [t0 and t1]

In the time interval amid t0 and t1, the primary switch "S" is in the ON condition. D_2, D_4, D_{input}, and D_{output} diodes act as a FB (forward bias). Equivalent circuits of mode 1 are represented in Figure 3. The main-side I_{Lk}* power increases gradually. The input voltage of the DC source will be delivered to Lm. The leakage inductor's power is present as the secondary side's energy is brought to C3 and nV_{L1} is the same as the voltage of the C_3. The output capacitor of 2 receives energy from the clamp capacitor 1. The first mode of operation is terminated at t is equal to t1.

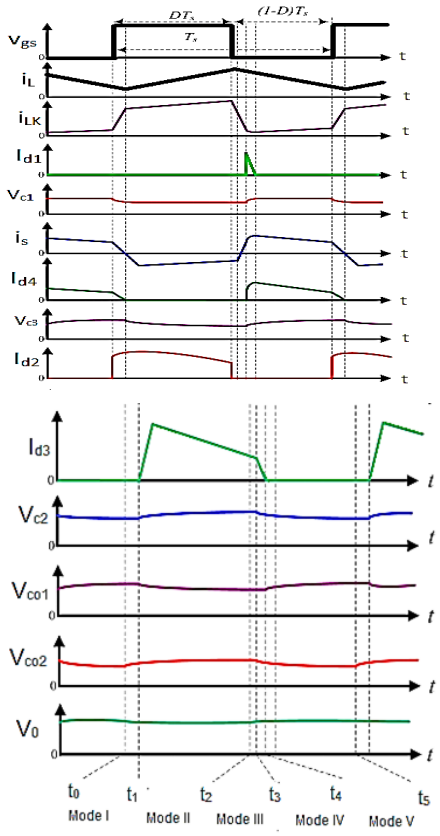

Figure 2. Voltage and Current Waveform of CCM mode of operation

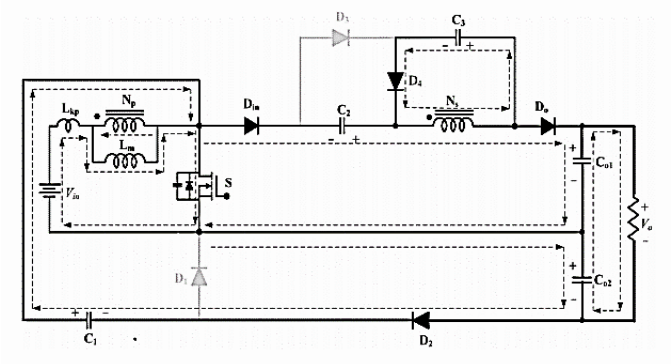

Figure 3. CCM mode I of operation

Mode 2 [t1 and t2]

In the time interval between t1 and t2, the primary switch "S" is in “ON” condition. The 3rd diode is FB. Corresponding circuitry of Mode number 2 is represented in Figure 4. The L_m (magnetizing-inductor) energy received from the input supply source The charge of capacitor 2 on the secondary side by using the CL and capacitor 3. The 1 and 2 outputs distribute their energy to load-unit. Second method of process, terminated at "t," is equal to t2.

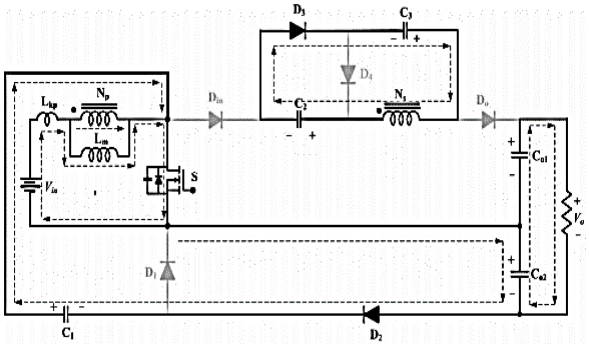

Figure 4. CCM mode II of operation

Mode 3 [t2 and t3]

Here, the primary switch ‘S’ is in the condition of being OFF and the 3rd diode acts as FB (forward bias). The mode 3 operation’s represented circuit is detailed in Fig 5. The primary switch "S" of the dependent capacitor is charged by L_k and L_m. Capacitor of 2 is charged by capacitor 3 and the coupledinductor. The output capacitance 1 and 2 delivered the energy for load.

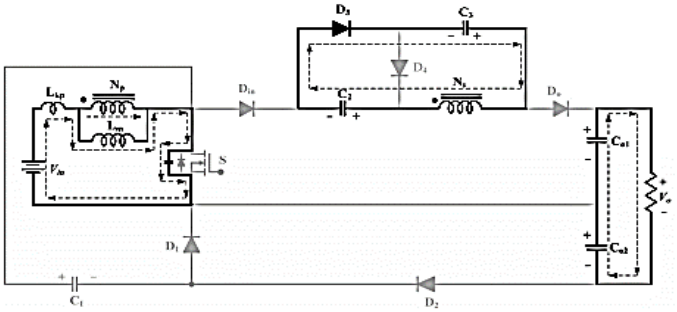

Figure 5. CCM mode III of operation

Mode 4 [t3 and t4]

Here, primary switch ‘S’ is in condition of OFF. The 1st and 3rd diodes act as a forward bias. The mode 4 operation’s corresponding circuitry is detailed in Fig 6. L_k and L_m based on the passive clamp capacitor 1 are charged, L_k is retrieved and I_{LK} is reduced. The fourth mode of operation is terminated at t and is equivalent to t4. The subordinate side’s power is equivalent to zero. The 3rd diode is in the condition of OFF but the diodes of 4, D_{in}, and D_o are in the condition of ON.

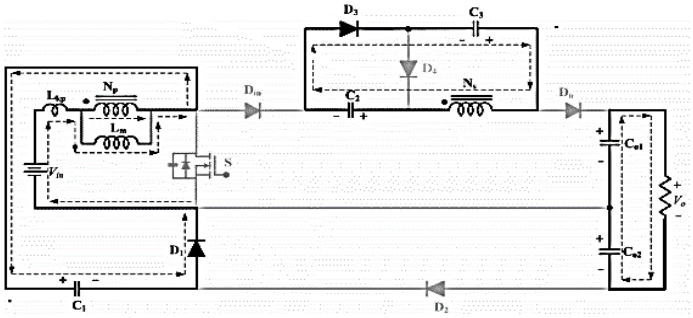

Figure 6.CCM mode IV of operation – Switch condition OFF

Mode 5 [t4 and t5]

The time interval of t is equal to t4. Switch 'S' is at condition "OFF". The 1st,4th diodes, D_{in} act as forward-bias. The mode 5 operation of the corresponding circuit is depicted in Fig 7. It is made up of coupledinductor, an input supply voltage, and a capacitor 2 to stream energy to outputvoltage capacitor 1, load. When t equals t5, mode 5 is terminated, and the primary switch "S" is set to ON from next-mode.

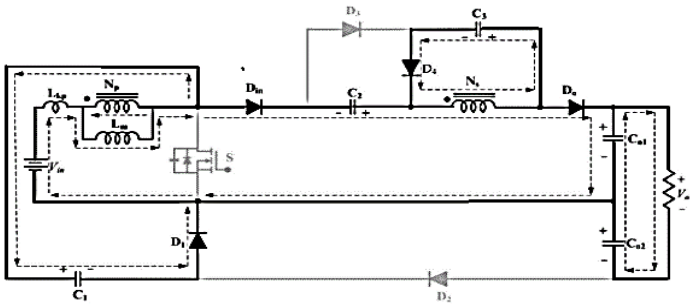

Figure 7. CCM mode V of operation – Switch turn off condition

B. Discontinuous-conduction mode

The discontinuous mode of operating voltage and current waveform is represented in fig 8. The L_k of the CI (coupled inductor) is not considered in discontinuous mode.

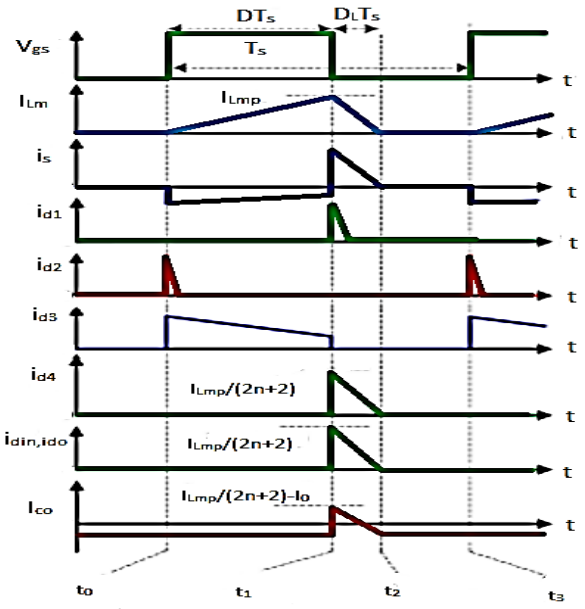

Figure 8. The discontinuous mode of operating voltage and the current waveform

Mode 1 [t0 and t1]

Here, primary switch 'S' at condition "ON", and the 1st and 3rd diodes act as forward-bias. The Mode 1 corresponding circuitry remains represented in Fig 9. As the primary current increased gradually, the Lm of the magnetising inductor received the power from the input of the DC supply. The secondary-side C_3 and CI (coupled inductor) provide energy to capacitor 2. The output capacitance of 1 and 2 delivers the energy for load circuit. Mode1 of operation is finished and the primaryswitch "S" is in the condition of being OFF (t = t1).

Mode 2 [t1 and t2]

Here, primary switch (S) at condition "OFF". The 1st and 4th diodes, D_{in} and D_o, act as forward-bias. The mode 2 operation's corresponding circuitry is represented in Fig. 10. L_m* and the DC supply's input power, capacitor 2, are excited by the input and output diodes, and power is delivered to C_{o1}.The L_m energy is delivered to capacitor of 3 by a coupled inductor. As t is equal to t2, mode 2 is terminated, and energy is warehoused in the magnetising inductor.

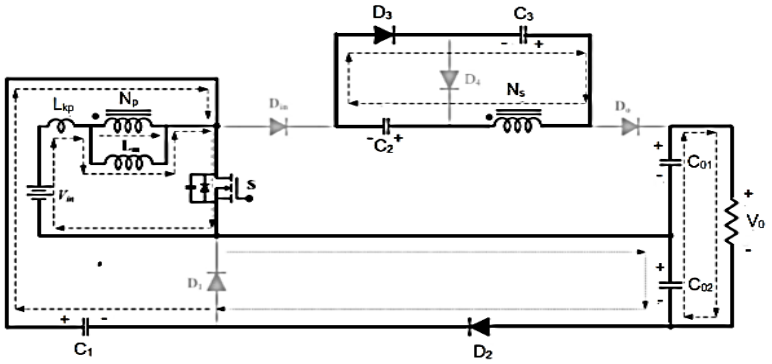

Figure 9. DCM mode I of operation

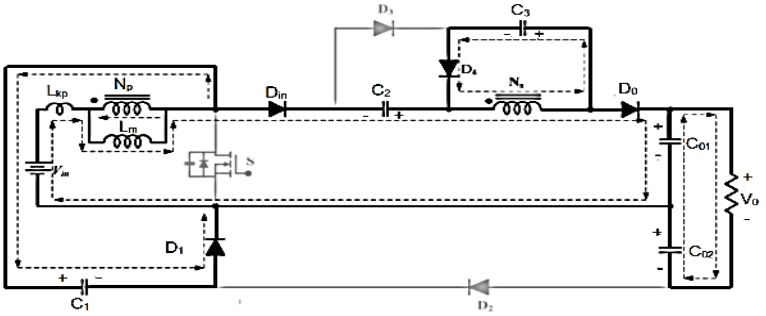

Figure 10. DCM mode II of operation

Mode 3 [t2 and t3]

In this case, primary switch "S" is turned off. Figure 11 shows how to operate itprocedures of the correspondent circuitry of mode 3 are represented in Fig 11. The C_{O1}, C_{O2} delivered energy for load circuits. t equals to t3. The mode 3 is terminated. The primary switch "S" is in the condition of being OFF from the next-mode.

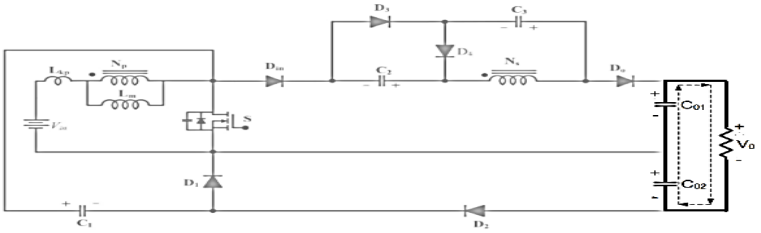

Figure 11. DCM mode III of operation

3. ANALYSIS OF STEADY STATE CONVERTER

3.1. Continuous-conduction mode

The turn's ratio has the definition as depicted in equation below:

$$n=\frac{N_S*}{N_P*} \quad (1)$$

The coupled inductor of couplingcoefficient k is stated as

$$k=\frac{L_m*}{L_m*+L_k*} \quad (2)$$

Due to shorttime durations, the operation of modes I, III, and IV is unnoticed. To streamline the steadystate analysis, the operations of modes II and V of continuous-conduction mode operation are measured. Operation of the II mode causes voltagestresses of VLK*, VL1*, and VL2*, as shown in Figure 3b.

$$V_{LK^*}^{11} = \frac{L_{k1^*}}{L_{m^*}+L_{k1^*}} V_{in} = (1\text{-}k^*)\ V_{in} \quad (3)$$

$$V_{L1^*}^{11} = \frac{L_{m^*}}{L_{m^*}+L_{k1^*}} V_{in} = \mathrm{k}^* V_{in} \quad (4)$$

$$\mathrm{V}_{\mathrm{L2}^*}^{11} = \mathrm{nV}_{\mathrm{L1}^*}^{11} = \mathrm{nkV_{in}} \quad (5)$$

The following I_k*,N_p* and N_s* equations are obtained from the volt-second balance principle

$$\int_0^{\mathrm{DT_s}} \mathrm{V}_{\mathrm{Lk}^*}^{11}\mathrm{dt} + \int_{\mathrm{DT_S}}^{\mathrm{T_s}} \mathrm{V}_{\mathrm{Lk}^*}^{\mathrm{V}}\mathrm{dt} = 0 \quad (6)$$

$$\int_0^{\mathrm{DT_s}} \mathrm{V}_{\mathrm{L1}^*}^{11}\mathrm{dt} + \int_{\mathrm{DT_S}}^{\mathrm{T_s}} \mathrm{V}_{\mathrm{L1}^*}^{\mathrm{V}}\mathrm{dt} = 0 \quad (7)$$

$$\int_0^{\mathrm{DT_s}} \mathrm{V}_{\mathrm{L2}^*}^{11}\mathrm{dt} + \int_{\mathrm{DT_S}}^{\mathrm{T_s}} \mathrm{V}_{\mathrm{L2}^*}^{\mathrm{V}}\mathrm{dt} = 0 \quad (8)$$

Substituting equation 3,4 and 5 into 6,7 and 8, the V_{Lk}*, V_{L1}* and V_0*at mode voltage can be represented by:

$$V_{LK^*}^{\mathrm{v}} = \frac{-D(1-k)^*}{(1-D)}\mathrm{V_{in}} \quad (9)$$

$$\mathrm{V}_{\mathrm{L1}^*}^{\mathrm{v}} = \frac{\mathrm{Dk}}{1-\mathrm{D}}\mathrm{V_{in}} \quad (10)$$

$$\mathrm{V}_{\mathrm{L2}^*}^{\mathrm{v}} = \frac{\mathrm{nDk}}{1-\mathrm{D}}\mathrm{V_{in}} \quad (11)$$

$$\mathrm{V_o^*} = 2\mathrm{V_{c1^*}} + \mathrm{V_{c2^*}} - \mathrm{V_{L2^*}^v} \quad (12)$$

In mode 2 capacitor 2 is charged and in mode 5 the capacitor 1 and 3 is charged. In basis of fig 3 (b) and 4 (c), the voltage stress capacitor 1,2 and 3 are represented as

$$V_{c3}^* = -V_{L2^*}^{\mathrm{v}} = \frac{nDk}{1-D} V_{in}^* \quad (13)$$

$$V_{c2}^* = V_{L2^*}^{11} + V_{c3}^* \quad (14)$$

Equation 5 and 13 are substituted into equation 14, the capacitor 1 and 2 of the voltage stress is expressed as:

$$V_{c2}^* = \frac{nk}{1-D} V_{in} \quad (15)$$

$$V_{c1}^* = V_{in}^* - V_{Lk^*}^V - V_{L1^*}^V = (1+\frac{Dk}{(1-D)}+\frac{D(1-k)}{(1-D)})V_{in}^* \quad (16)$$

Equation 11 and 15, 16 substituting into 12, voltage gain is expressed as:

$$M_{CCM}^* = \frac{V_0^*}{V_{in}^*} = \frac{2+nk+nDk^*}{(1-D)} \quad (17)$$

When considering k = 1, leakageinductor of coupledinductor is abandoned.

When considering k equals to 1 the idealgain of the voltage is expressed as

$$M_{CCM}^* = \frac{(2+n+nD)}{(1-D)} \quad (18)$$

The proposed converter duty cycle and voltage gain and the conventional converter's incessant transmission mode of process are represented in figures 12 and Table-1. The projected converter voltage gain is superior to the existing converter without changing the duty cycle. This converter achieves a higher boost stepper-up ratio and better efficacy compared to the existing converters, except [9] and [29] converters. The [9] converter has a greater efficiency, but the drawback of this converter is the high voltage stress problem.

Peak voltage is maximum in off mode condition. The coupled inductor is large in size. When compared to proposedconverter, [29] converter has a lower efficiency and a lower Vmax.

3.2. Discontinuous-conduction mode

In the three modes of the discontinuous mode of operation, the volt and current waveforms of primary apparatuses are revealed in Fig. 5. The proposed converter's various modes of operation in the discontinuous mode are revealed in Fig.6. The primary switch 'S' is in the ON position in mode 1 of operation, as illustrated in fig. 6(a).The stress voltage of inductor 1 and 2 is represented as

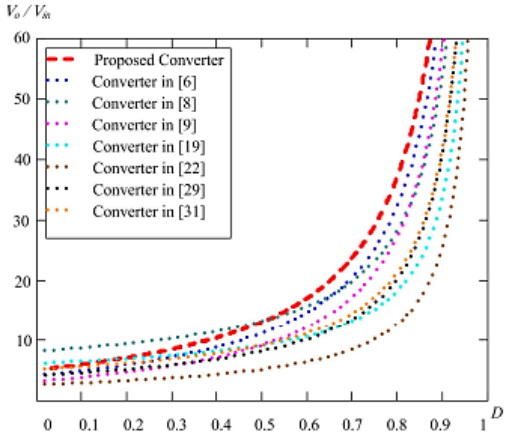

Figure.12. Voltage increases of new High Gain Converter

$$V_{L1}^{l} = V_{in}^{*} \tag{19}$$

$$V_{L2}^{l} = nV_{in}^{*} \tag{20}$$

The crowning current of L_{mp} is stated as

$$IL_{mp} = \frac{V_{in}^{*}}{L_{m}^{*}} DT_s \tag{21}$$

Capacitance of 2 and output capacitance 1 and 2 are represented as

$$V_{c2}^{*} = V_{L2}^{l} + V_{c3}^{*} \tag{22}$$

$$V_{co2}^{*} = V_{c1}^{*} \tag{23}$$

$$V_{co}1^{*} = V_{0}^{*} - V_{c1}^{*} \tag{24}$$

In mode 2 operation the primary switch S is off condition. In mode 2 operation the voltage stresses are represented as

$$V_{L1^{*}}^{11} = V_{in}^{*} - V_{cl}^{*} \tag{25}$$

$$V_{L2^{*}}^{11} = 2V_{c1} + V_{c2} - V_{0} \tag{26}$$

$$V_{L2^{*}}^{11} = -V_{c3}^{*} \tag{27}$$

In mode-3 operation, primary switch 'S' is at condition OFF. Output capacitance of 1 and 2 provide energy to load. Inductive voltage of 1 and 2 are represented as:

$$V_{L1^{*}}^{111} = V_{L2^{*}}^{111} = 0 \tag{28}$$

In coupled inductor, the volt-second balance principle are applied

$$\int_0^{DT_s} V_{L1^*}^1 dt + \int_{DT_s}^{(D+D_L)T_s} V_{L1^*}^{11} dt + \int_{(D+D_L)T_s}^{T_s} V_{L2^*}^{111} dt = 0 \quad (29)$$

$$\int_0^{DT_s} V_{L2^*}^1 dt + \int_{DT_s}^{(D+D_L)T_s} V_{L2^*}^{11} dt + \int_{(D+D_L)T_s}^{T_s} V_{L2^*}^{111} dt = 0 \quad (30)$$

Equation 20,27 and 28 are substituting into equation 30, the voltage across the capacitor 3 are represented as:

$$V_{c3}* = \frac{nD}{D_L} V_{in}* \quad (31)$$

Same like, equation 19,25and 28 are substituting into 29, 22 and 27,28 into 30 the capacitor of 1 and 2 voltage stress are represented as:

$$V_{c1}* = \frac{D+D_L^*}{D_L^*} V_{in}* \quad (32)$$

$$V_{c2}* = (n+\frac{nD}{D_L}) V_{in}* \quad (33)$$

The equation of 20,26,28,32 and 33 are substituting into 30 the proposed converter gain of the voltage is obtained from discontinuous mode of operation are represented as:

$$V_o* = [\frac{2D}{D_L}(1+n)+(n+2)]V_{in}* \quad (34)$$

$$D_L = \frac{2D(1+n)Vin*}{V_o-(2+n)Vin*} \quad (35)$$

In fig 5, the average current is represented by

$$i_{co1} = \frac{1}{2} DL\frac{I_{Lmp}^*}{2+2n} - I_o* \quad (36)$$

The current of the output capacitor 1 is zero for steady state analysis and 21, 35 and i_{co1} is equal to zero's are substituted in equation 36.

Therefore

$$\frac{D^2(n+1)V_{in}^{2}* T_s}{[V_o^*-(n+2)V_{in}^*].(2n+2).L_m} = \frac{V_o^*}{R} \quad (37)$$

The magnetic inductance of the time constant is defined as

$$\tau_{Lm}^* = \frac{L_m^*}{RT_s^*} \quad (38)$$

Table 1. Proposed converter compared with Conventional Converters

Name of the Converters	Quantity of Components	ηmax	VInput*/VOutput*	Gain of the Voltage (M*CCM = VOutput*/VInput*)
High Gain Converter	6 Diodes 5 Capacitor	96.4%	Vin = 24 V Vo = 410V	$M_{CCM}^* = \frac{2+n+nD}{(1-D)}$
[6]	3 Diodes 3 Capacitor	-	Vin = 48 V Vo = 380V	$M_{CCM}^* = \frac{1+n}{1-D}$
[8]	4 Diodes 4 Capacitor	95.8%	Vin = 24 V Vo = 400V	$M_{CCM}^* = \frac{1+n+nD}{1-D}$
[9]	4 Diodes 4 Capacitor	96.7%	Vin = 24 V Vo = 400V	$M_{CCM}^* = \frac{2+n}{1-D} + n$
[19]	4 Diodes 5 Capacitor	95.7%	Vin = 24 V Vo = 200V	$M_{CCM}^* = n\frac{1+D}{1-D}$
[22]	5 Diodes 3 Capacitor	96.2%	Vin = 24 V Vo = 200V	$M_{CCM}^* = \frac{n(2-D)}{(1-D)}$
[29]	5 Diodes 3 Capacitor	96.5%	Vin = 35 V Vo = 200V	$M_{CCM}^* = \frac{2+n}{2(1-D)}$
[31]	3 Diodes 3 Capacitor	95.2%	Vin = 36.5 V Vo = 200V	$M_{CCM}^*(1+n)+\frac{1}{(1-D)}+\frac{D}{(1-D)}n$

Equation 38 is substituting in equation 37, the voltage gain is obtained as follows

$$M^*_{DCM}=\frac{V^*_0}{V^*_{in}}=\frac{2n+2}{2}+\sqrt{\frac{(2n+2)^2}{4}+\frac{D^2(n+1)}{(2n+2).\tau^*_{Lm}}} \quad (39)$$

3.3. The CCM and DCM Boundary- Condition

For the higher Gain converters CCM and DCM, the edge-condition mode of power improvement is same. Equation 18 and 39 based time-constant of the L is expressed as

$$\tau^*_{LmB}=\frac{\frac{D^2(n+1)}{2n+2}}{[\left(\frac{2+n+nD}{1-D}\right)-\frac{2n+2}{2}]^2-\frac{(2n+2)^2}{4}} \quad (40)$$

Boundary condition of Duty cycle and τ^*_{LmB} is represented in fig.13. The τ is greater than the iLmB the converter operates like CCM otherwise DCM.Table 1 represents the comparison of proposed converter with other conventional converters. The maximum efficiency obtained for the proposed converter is 96.4% which is much higher than the other conventional converters. Table 2 represents the voltage stress comparison with existing methods.

Table 2. Comparison Table for Voltage Stress

Comparison	Switch Drain-Source Voltage (V)	
	Formula	Vin=24, Vo =380, n=3
Proposed		
[13]	Vo/(1+n)	95
[14]	2Vo/(n+2)	152
[15]	Vo/(n+2)	76

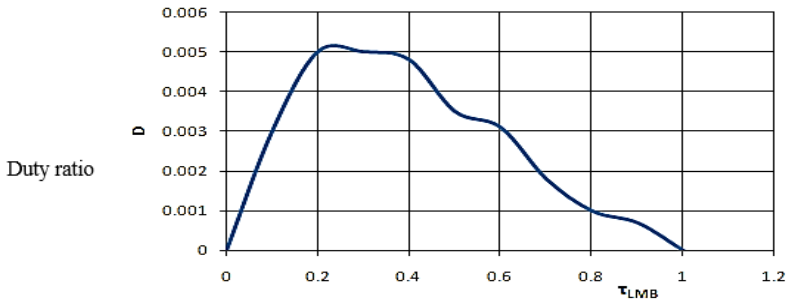

Figure 13. The High Gain Converter boundary condition n=3

4. THE DESIGN PROCEDURE OF HIGH GAIN CONVERTER

The recital of projected converter at 150 W to be tested and measured. The specification of projected converter is as mentioned below and verify the performance of the proposed converter, a prototype of the basic structure circuit is implemented in the laboratory.

V_{in}*- Input-direct current voltage: 24V
V_{out}*- Output-direct current voltage: 410V
P_{max}* – Extreme production power: 150W
F_s*– Switch frequency: 50 KHZ
S – Switch: IXTH130N10T1
D – diodes-D_1,D_2 and D_3: DSEI-30-10A: D_{input} and D_4: 25JPE401
C- capacitors-C_1*& C_{co2}*: 100 µF/100 Volt, C_2: 100 µF/250 Volt, C_3: 100 µF/100 Volt, and C_{o1}: 220 µF/400 Volt aluminium- capacitors
T- Transformer- ETDI-49 core PC*-32, Np*: N_s* = 1:3, L_m* = 32 µH and L_k* = 0.22 µH; k = 0.993.

The subordinate current and I_{LK}* V_{DS} of the primary switch under full load condition P_o* = 150W, input voltage is 24 V is represented in fig. 14 (a). The incessant conduction mode of process when the switch is at condition ON, no current flowsthrough the proposed circuit. Coupled-inductor's subordinate power waveform is represented in Fig 14 (b).

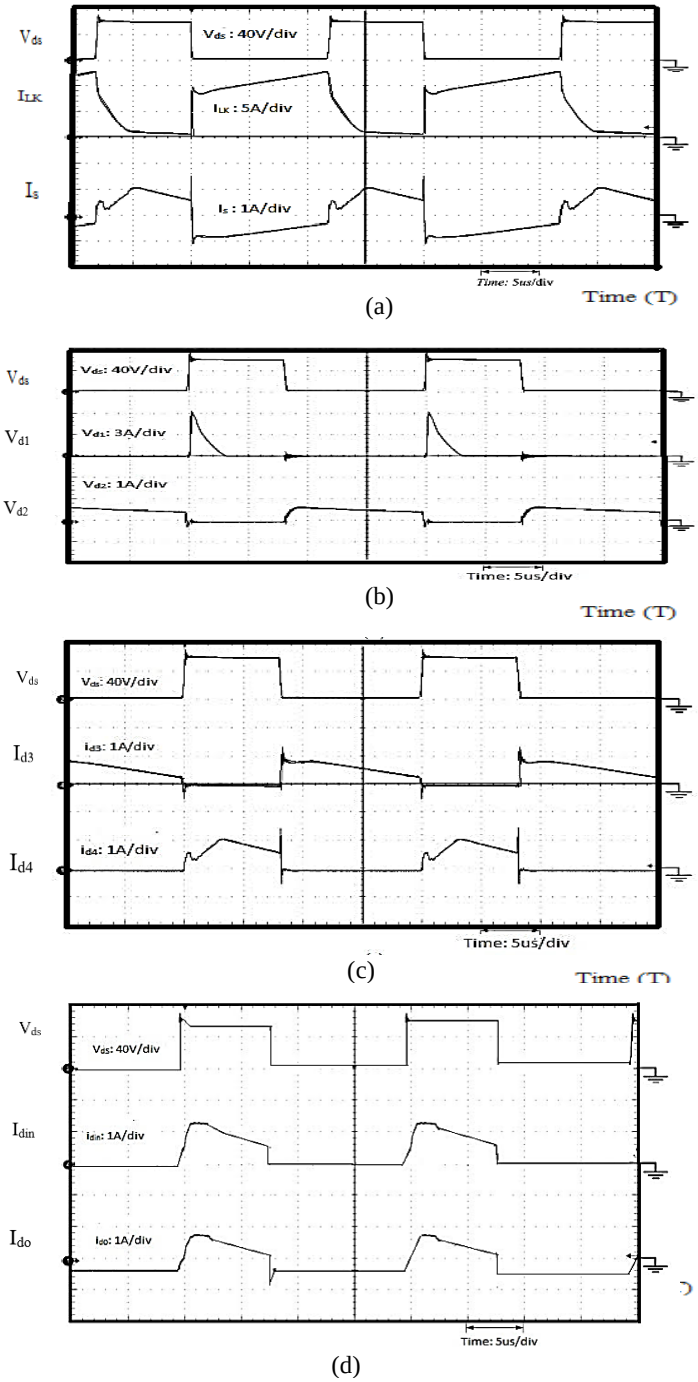

Figure 14. Full Load Condition experimental waveform output power P_o*= 150W

The I_{c1} is transferred to the diode 2, and the amount of energy is transferred to output capacitor 2 when switch "S" is in ON condition. When switch "S" is turned off, energy is absorbed in capacitor C1 from the input voltage and the parasitic capacitor. For the diode and for charging the capacitor, the voltage is absorbed from the input voltage and subordinate-side of the coupled-inductor waveforms as represented in Fig. 14 (c). The diode's input and output current waveforms are illustrated in Fig. 14 (d). The input voltage energy, though an input to the capacitor, is delivered to the stepper-up circuitry and is transferred to the D output. The output voltage capacitor 1,2, and 3 is represented in fig. 15 (a). It satisfies the equations 14,15, and 17. The CV_{in} and CV_{out} are represented in fig. 15 (b). The proposed converter efficiency at 150 W loads and max is 96.4%, as represented in fig 16. The output voltage waveform obtained from the prototype is illustrated in fig. 18. Load step change occurred during simulation is illustratd in Fig 19. Fig 20 and 21 depicts the leakage inductor current and diode output current obtained from the proposed model.

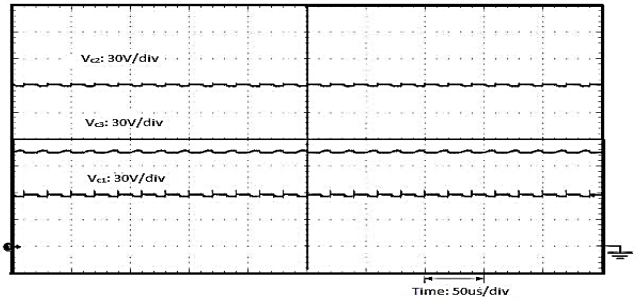

Figure 15 (a). Full Load Condition experimental output voltage capacitor

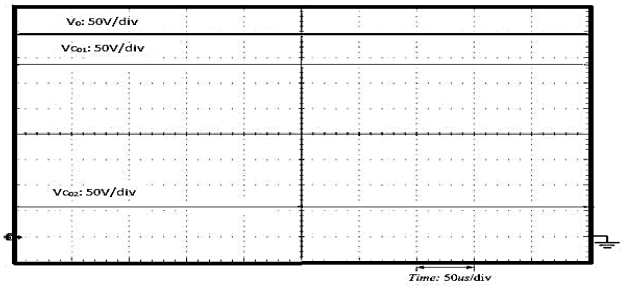

Figure 15 (b). Full Load Condition experimental CV_{in} and CV_{out} waveform output power Po*= 150W.

The experimental prototype of proposed converter is shown in Fig. 17.

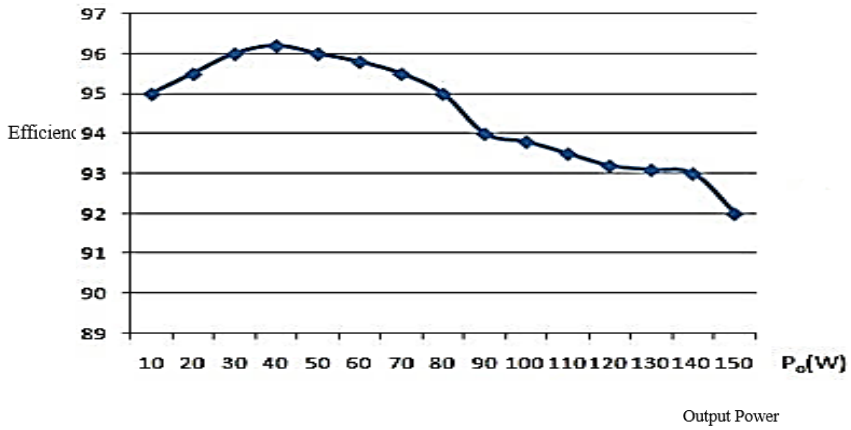

Figure 16. The proposed converter efficiency at 150W loads

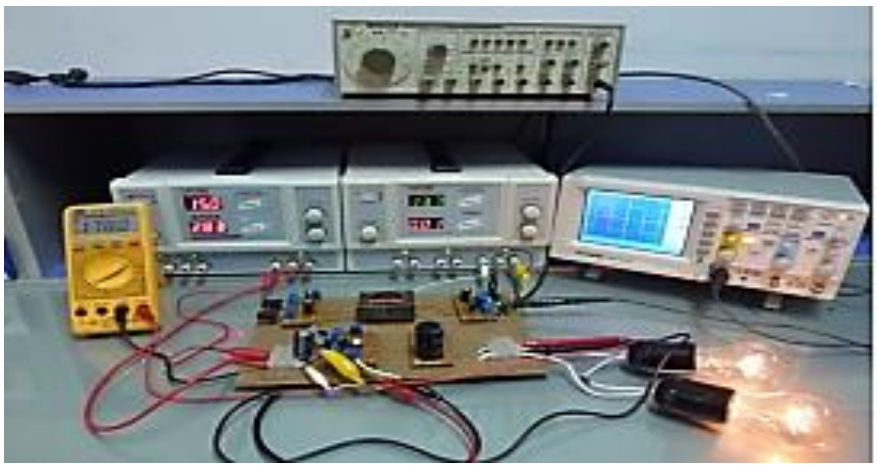

Figure 17. Experimental 150 W prototype in laboratory

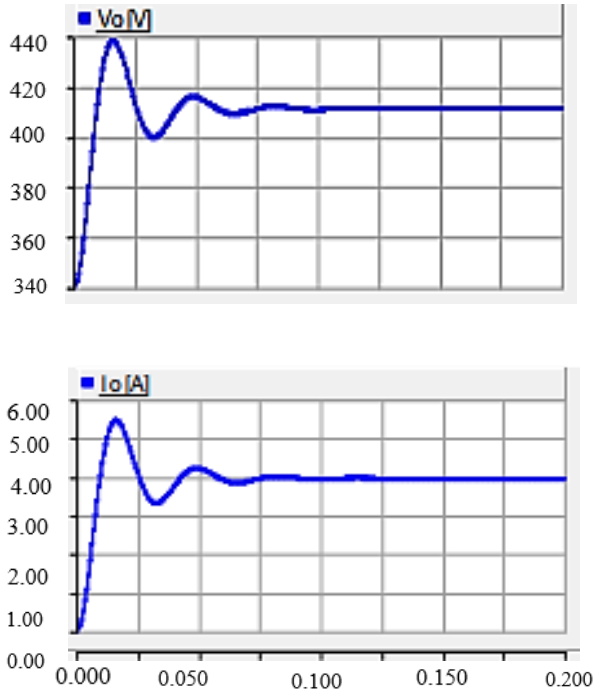

Figure 18.Simulated output voltage and current.0.30

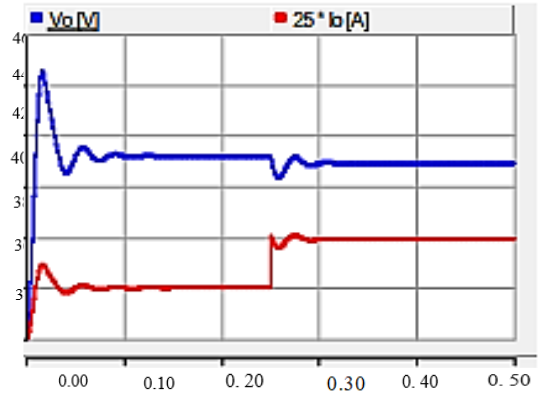

Figure 19. Change in Load

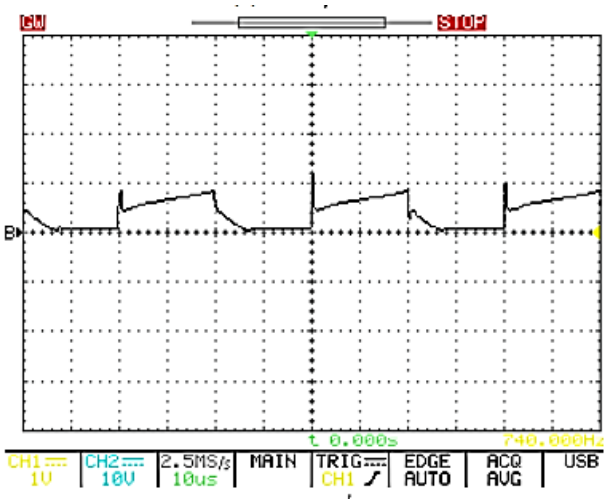

Figure 20. Leakage inductor current i_{Lk}^{*}

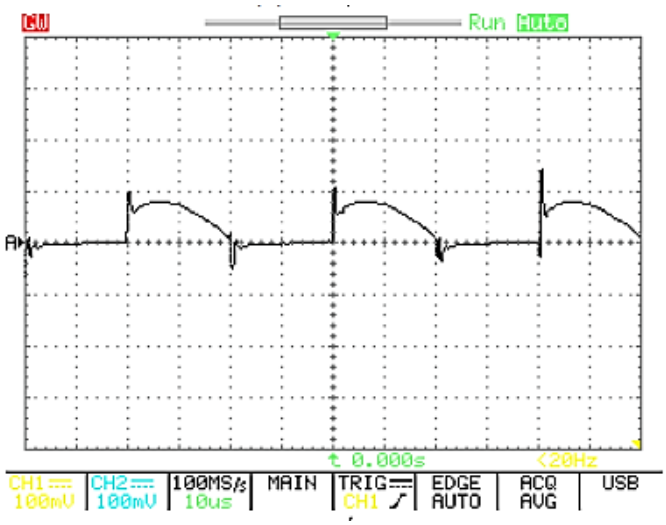

Figure 21. Diode output current i_{Do}

5. CONCLUSIONS

The converter was successfully integrated using high gain step-up circuits and coupled-inductor. The capacitor charged and discharged based on high-voltage gain was successfully achieved. Without a high duty cycle, a high stepper-up volt gain is achieved by using a coupled-inductor and a capacitor. Clamp circuitry is utilised to resolve energy loss from outflow inductance and minimise switch voltage spike problems. The switching loss was reduced by using fewer voltage-stress components and a minimum conducting resistance Rds. The proposed converter prototype was constructed with Vin 24Vinto 410V and Pmax = 150W to get a maximum efficiency of almost 96.4% and minimise the switching losses.

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