PV Systems based High Gain Converter using CI and SCC Techniques

S.Sankarananth¹, P.Sivaraman²

¹Department of Electrical and Electronics Engineering, Excel College of Engineering and Technology, Komarapalayam Anna University, Tamilnadu, India.
²Department of Electrical and Electronics Engineering, Bannari Amman Institute of Technology, Anna University, Sathyamangalam, Tamilnadu, India.

ABSTRACT

In this paper, new techniques for a CI (coupled inductor) and SCC (Switched Clamp Capacitor)-based stepup higher-level voltage DC-DC converter were implemented. The CI and SC, charge and discharge the energy, respectively, to attain higher gains. Using the clamp circuitry, the stress on the switching volt level and inductance leakage are removed. The reversed retrieval problem in the diode was eradicated with the help of a coupled inductor (CI). The new topology is to get more gain from the voltage and improve efficacy. The steadystate examination of novel DC-DC converter operation procedures are discussed here. The proposed model has an inputvoltage of 24V and an outputvoltage of 410V. Pmax of 150W was given to get a maximum of 96.4%.

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Corresponding Author:
S.Sankarananth
Department of Electrical and Electronics Engineering, Excel College of Engineering and Technology, Komarapalayam - 637303
Anna University, Tamilnadu, India.
Email: sankarananth.ecet@excelcolleges.com

1. INTRODUCTION

Our country is deeply concerned about the energy crisis and environmental issues [1]. In this concern, the global warming problem will occur, and this will in turn increase the level of the sea by about 2 meters. This has a greater impact on the lives of all human beings. Non-conventional energy sources are used to solve the air pollution and energy crises and global warming problems. Non-conventional Energy causes like sun_energy, energy from the wind, and wave_energy is widely used. [2], [3], [4]. Non-conventional energy sources produce a lower voltage level and it must be increased by using a converter named stepper-up boost DC-DC. This higher voltage output is transferred through the inverter to convert DC into AC [5] [6] [7] [8].

The stepper-up boost DC-DC converter ratio disturbs entire system efficacy. The existing converter circuit topology is not suitable for Steper-Up Boost dc-to-dc converter ratio applications. In existing Stepper-Up Boost dc-to-dc converter circuit, the duty cycle is increased to 1. During ideal conditions, the Stepper-Up boosting conversion ratio should reach its maximum value. The Stepper-Up Boost DC-DC Converter circuits EMI and Converse retrieval problems are issued to limit the high voltage gain by using the C, L, R, and switches. The leakage of the transformer affects the huge amount of power dissipation and a large amount of voltage spike problems occur on switch.

Selection of power switches with high voltage stress is the main consideration because of redundant cost and more space problems. To introduce the new architecture, the existing method of the boost converter circuit problems is overcome. The new architecture of the switched capacitor [9], [10], [11], [12], [13] coupled inductor [14 to 21], and lifting of voltage techniques [22] [23] are proposed. The minimum amount of energy strain in switching circuits with an upsurge in alteration ratio of voltage is achieved by using an inductive structure of a coupled inductance stepper-up boosting converter circuit. This type of technique is mostly used,
but the main disadvantage of these techniques is the leakage inductance of the CI and spikes in voltage. The snubber circuit is used to solve issues like leakage inductance and spikes in voltage. A higher stepper-up boosting ratio function is attained by using techniques of a switched-capacitor and boost of voltage techniques, but more transient current and conduction losses occur on the chief switch. In this case, switch ‘S’ will be turned on, and in turn, a switch-based capacitor will be utilised to back up the energy. When power volt is zero, energy stored in capacitor-unit is utilised for discharging energy back to the load-unit. Lift of voltage techniques are similar to a SEPIC converter or a CUK converter in terms of energy transfer from L-C-L. This energy transfer from the inductor to the capacitor affects the current stress on the capacitor. [24] [25]. The boost stepper-up flyback converter-based switch capacitor techniques produce a huge amount of step-up ratio. In this technique, the switch is ON condition that the boost converter starting stage is the same as the amalgamation of the booster-based converter with SC. The turned-off mode of the switch represents the 2nd stage of the boost converter, and the same is similar to the combination of fly back with an SCC [26 to 37]. The proposed method of adjusting the duty cycle can reach a maximum boost. By using the clamp circuit to produce high efficiency, we can minimise the leakage inductance of the energy recovery from the CI (coupled inductor). A large voltage gain can be achieved without operating at extreme duty cycles, that is ideal for renewables. A single current switch is simple to operate for the appropriate output volts, generality capability is required. A passively voltage clamping circuit that reduces overvoltage on the switch, recovers inductance leakage energy, and boosts a converter’s voltage output. It will resolve the issue of diode reversal restoration. The switching loss was reduced by using fewer voltage-stress components and a minimum conducting resistance Rds and to get a maximum efficiency of almost 96.4%.

2. HIGH GAIN CONVERTER CONVERTER

The new high gain converter circuit consists of the input voltage of a DC supply, the primary switch S, coupled inductors Np and Ns as represented below in Figure 1. V1 and V2 are the RMS voltages at the input and output of RC correspondingly.

Figure 1. Planned Converter Circuitry

Clamp circuit consists of the diodes D1, D2 and C1. The Stepper-Up boost-circuitry consists of D3 and D4 diodes, capacitors of C2 and C3. The coupled inductor equal circuits consist of Ls (leakage inductor) and Lm (magnetics inductor) and the primary and secondary windings turns Np and Ns of the ideal transformer. The proposed converter operating principle and the below conditions are considered

- C1, C2, and C3 capacitors, as well as C01 and C02, are adequately large.
- Capacitor voltages Vc1, Vc2, and Vc3, assumed to be constant.
- Consider power devices as ideal components, with parasitic capacitors neglected.
- The coupling inductor K’s co-efficient is the same as Lm*/(Lm*+Lk*).
- n (ratio of turns) = Ns*/Np*
The two-mode operator procedures of the projected converter

- Continuous Conduction Mode
- Discontinuous Conduction Mode

A. Continuous Conduction Mode

Continuous Conduction Mode of operation’s voltage and power waveform is represented in Figure 2. Five operating modes of continuous-conduction are:

I Mode \([t_0 \text{ and } t_1]\)

In the time interval amid \(t_0\) and \(t_1\), the primary switch “S” is in the ON condition. \(D_2, D_3, D_{\text{output}}\), and \(D_{\text{output}}\) diodes act as a FB (forward bias). Equivalent circuits of mode 1 are represented in Figure 3. The main-side \(I_{L1}\) power increases gradually. The input voltage of the DC source will be delivered to \(L_m\). The leakage inductor’s power is present as the secondary side’s energy is brought to \(C_3\) and \(nV_{L1}\) is the same as the voltage of the \(C_3\). The output capacitor of 2 receives energy from the clamp capacitor 1. The first mode of operation is terminated at \(t = t_1\).

![Figure 2. Voltage and Current Waveform of CCM mode of operation](image)

![Figure 3. CCM mode 1 of operation](image)
Mode 2 [t1 and t2]
In the time interval between t1 and t2, the primary switch "S" is in “ON” condition. The 3rd diode is FB. Corresponding circuitry of Mode number 2 is represented in Figure 4. The \( L_m \) (magnetizing-inductor) energy received from the input supply source The charge of capacitor 2 on the secondary side by using the CL and capacitor 3. The 1 and 2 outputs distribute their energy to load-unit. Second method of process, terminated at “t,” is equal to t2.

![Figure 4. CCM mode II of operation](image)

Mode 3 [t2 and t3]
Here, the primary switch ‘S’ is in the condition of being OFF and the 3rd diode acts as FB (forward bias). The mode 3 operation’s represented circuit is detailed in Fig 5. The primary switch "S" of the dependent capacitor is charged by \( L_k \) and \( L_m \). Capacitor of 2 is charged by capacitor 3 and the coupled-inductor. The output capacitance 1 and 2 delivered the energy for load.

![Figure 5. CCM mode III of operation](image)

Mode 4 [t3 and t4]
Here, primary switch ‘S’ is in condition of OFF. The 1st and 3rd diodes act as a forward bias. The mode 4 operation’s corresponding circuitry is detailed in Fig 6. \( L_k \) and \( L_m \) based on the passive clamp capacitor 1 are charged, \( L_k \) is retrieved and \( I_{LK} \) is reduced. The fourth mode of operation is terminated at t and is equivalent to t4. The subordinate side’s power is equivalent to zero. The 3rd diode is in the condition of OFF but the diodes of 4, \( D_{in} \), and \( D_o \) are in the condition of ON.

![Figure 6. CCM mode IV of operation – Switch condition OFF](image)
Mode 5 \([t_4 \text{ and } t_5]\)

The time interval of \(t\) is equal to \(t_4\). Switch ‘S’ is at condition “OFF”. The 1st, 4th diodes, \(D_m\) act as forward-bias. The mode 5 operation of the corresponding circuit is depicted in Fig 7. It is made up of coupledinductor, an input supply voltage, and a capacitor 2 to stream energy to outputvoltage capacitor 1, load. When \(t\) equals \(t_5\), mode 5 is terminated, and the primary switch "S" is set to ON from next-mode.

![Figure 7. CCM mode V of operation – Switch turn off condition](image)

**B. Discontinuous-conduction mode**

The discontinuous mode of operating voltage and current waveform is represented in fig 8. The \(L_k\) of the CI (coupled inductor) is not considered in discontinuous mode.

![Figure 8. The discontinuous mode of operating voltage and the current waveform](image)

Mode 1 \([t_0 \text{ and } t_1]\)

Here, primary switch ‘S’ at condition “ON”, and the 1st and 3rd diodes act as forward-bias. The Mode 1 corresponding circuitry remains represented in Fig 9. As the primary current increased gradually, the \(L_m\) of the magnetising inductor received the power from the input of the DC supply. The secondary-side \(C_3\) and CI (coupled inductor) provide energy to capacitor 2. The output capacitance of 1 and 2 delivers the energy for load circuit. Mode1 of operation is finished and the primaryswitch "S" is in the condition of being OFF (\(t = t_1\)).

Mode 2 \([t_1 \text{ and } t_2]\)

Here, primary switch (S) at condition “OFF”. The 1st and 4th diodes, \(D_m\) and \(D_o\) act as forward-bias. The mode 2 operation’s corresponding circuitry is represented in Fig. 10. \(I_m\) and the DC supply’s input power, capacitor 2, are excited by the input and output diodes, and power is delivered to \(C_1\). The \(L_m\) energy is delivered to capacitor of 3 by a coupled inductor. As \(t\) is equal to \(t_2\), mode 2 is terminated, and energy is warehoused in the magnetising inductor.
Mode 3 [t2 and t3]

In this case, primary switch "S" is turned off. Figure 11 shows how to operate if procedures of the correspondent circuitry of mode 3 are represented in Fig 11. The $C_{O1}$, $C_{O2}$ delivered energy for load circuits. $t$ equals to t3. The mode 3 is terminated. The primary switch "S" is in the condition of being OFF from the next-mode.

3. ANALYSIS OF STEADY STATE CONVERTER

3.1. Continuous-conduction mode

The turn’s ratio has the definition as depicted in equation below:

$$n = \frac{N_s}{N_p}$$  \hspace{1cm} (1)

The coupled inductor of coupling coefficient k is stated as

$$k = \frac{l_{m^*}}{l_{m^*} + l_{k^*}}$$  \hspace{1cm} (2)

Due to shorttime durations, the operation of modes I, III, and IV is unnoticed. To streamline the steadystate analysis, the operations of modes II and V of continuous-conduction mode operation are measured. Operation of the II mode causes voltage stresses of $V_{LK^*}$, $V_{L1^*}$, and $V_{L2^*}$, as shown in Figure 3b.

$$V_{LK^*}^{11} = \frac{l_{k^*}}{l_{m^*} + l_{k^*}} V_{in} = (1-k^*) V_{in}$$  \hspace{1cm} (3)
\[
V_{L1}^{11} = \frac{L_{m}^{*}}{L_{m}^{*} + L_{k1}^{*}} V_{in} = k^{*} V_{in} \tag{4}
\]
\[
V_{L2}^{11} = nV_{L1}^{11} = nkV_{in} \tag{5}
\]

The following \( L_{k}^{*}, N_{p}^{*} \) and \( N_{s}^{*} \) equations are obtained from the volt-second balance principle

\[
\int_{0}^{T_{S}} V_{Lk}^{11} dt + \int_{0}^{T_{S}} V_{Lk}^{V} dt = 0 \tag{6}
\]
\[
\int_{0}^{T_{S}} V_{L1}^{11} dt + \int_{0}^{T_{S}} V_{L1}^{V} dt = 0 \tag{7}
\]
\[
\int_{0}^{T_{S}} V_{L2}^{11} dt + \int_{0}^{T_{S}} V_{L2}^{V} dt = 0 \tag{8}
\]

Substituting equation 3, 4 and 5 into 6, 7 and 8, the \( V_{Lk}^{*}, V_{L1}^{*} \) and \( V_{0}^{*} \) at mode voltage can be represented by:

\[
V_{Lk}^{*} = \frac{-D(1-k)^{*}}{1-D} V_{in} \tag{9}
\]
\[
V_{L1}^{*} = \frac{Dk}{1-D} V_{in} \tag{10}
\]
\[
V_{L2}^{*} = \frac{nDk}{1-D} V_{in} \tag{11}
\]
\[
V_{0}^{*} = 2V_{c1}^{*} + V_{c2}^{*} + V_{L2}^{*} \tag{12}
\]

In mode 2 capacitor 2 is charged and in mode 5 the capacitor 1 and 3 is charged. In basis of fig 3 (b) and 4 (c), the voltage stress capacitor 1, 2 and 3 are represented as

\[
V_{c3}^{*} = -V_{L2}^{*} = \frac{nDk}{1-D} V_{in}^{*} \tag{13}
\]
\[
V_{c2}^{*} = V_{L2}^{11} + V_{c3}^{*} \tag{14}
\]

Equation 5 and 13 are substituted into equation 14, the capacitor 1 and 2 of the voltage stress is expressed as:

\[
V_{c2}^{*} = \frac{nk}{1-D} V_{in} \tag{15}
\]
\[
V_{c1}^{*} = V_{in}^{*} - V_{Lk}^{*} - V_{L1}^{*} = (1+\frac{Dk}{1-D}) V_{in}^{*} \tag{16}
\]

Equation 11 and 15, 16 substituting into 12, voltage gain is expressed as:

\[
M_{CCM}^{*} = \frac{V_{L2}^{*}}{V_{in}^{*}} = \frac{2+nk+nDk^{*}}{1-D} \tag{17}
\]

When considering \( k = 1 \), leakage inductor of coupled inductor is abandoned.

When considering \( k \) equals to 1 the ideal gain of the voltage is expressed as

\[
M_{CCM}^{*} = \frac{(2+n+D)}{(1-D)} \tag{18}
\]

The proposed converter duty cycle and voltage gain and the conventional converter’s incessant transmission mode of process are represented in figures 12 and Table 1. The projected converter voltage gain is superior to the existing converter without changing the duty cycle. This converter achieves a higher boost step-up ratio and better efficacy compared to the existing converters, except [9] and [29] converters. The [9] converter has a greater efficiency, but the drawback of this converter is the high voltage stress problem.
Peak voltage is maximum in off mode condition. The coupled inductor is large in size. When compared to proposed converter, [29] converter has a lower efficiency and a lower $V_{\text{max}}$.

### 3.2. Discontinuous-conduction mode

In the three modes of the discontinuous mode of operation, the volt and current waveforms of primary apparatuses are revealed in Fig. 5. The proposed converter’s various modes of operation in the discontinuous mode are revealed in Fig. 6. The primary switch 'S' is in the ON position in mode 1 of operation, as illustrated in fig. 6(a). The stress voltage of inductor 1 and 2 is represented as

$$V_{L1}^* = V_{\text{in}}^*$$  \hspace{1cm} (19)

$$V_{L2}^* = nV_{\text{in}}^*$$  \hspace{1cm} (20)

The crowning current of $L_{\text{mp}}$ is stated as

$$I_{L_{\text{mp}}} = \frac{V_{\text{in}}^*}{l_{\text{in}}} DT_s$$  \hspace{1cm} (21)

Capacitance of 2 and output capacitance 1 and 2 are represented as

$$V_{c2}^* = V_{L2}^* + V_{c3}^*$$  \hspace{1cm} (22)

$$V_{o2}^* = V_{c1}^*$$  \hspace{1cm} (23)

$$V_{o1}^* = V_0^* - V_{c1}^*$$  \hspace{1cm} (24)

In mode 2 operation the primary switch S is off condition. In mode 2 operation the voltage stresses are represented as

$$V_{L1}^{11} = V_{\text{in}}^* - V_{c1}^*$$  \hspace{1cm} (25)

$$V_{L2}^{11} = 2V_{c1} + V_{c2} - V_0$$  \hspace{1cm} (26)

$$V_{L2}^{11} = -V_{c3}^*$$  \hspace{1cm} (27)

In mode-3 operation, primary switch 'S' is at condition OFF. Output capacitance of 1 and 2 provide energy to load. Inductive voltage of 1 and 2 are represented as:

$$V_{L1}^{111} = V_{L2}^{111} = 0$$  \hspace{1cm} (28)

In coupled inductor, the volt-second balance principle are applied
\[
\int_0^{T_s} V_{L1}^1 dt + \int_0^{(D+D_L)T_s} V_{L1}^{11} dt + \int_0^{T_s} V_{L2}^{11} dt = 0
\]  
(29)

\[
\int_0^{T_s} V_{L2}^1 dt + \int_0^{(D+D_L)T_s} V_{L2}^{11} dt + \int_0^{T_s} V_{L2}^{11} dt = 0
\]  
(30)

Equation 20, 27 and 28 are substituting into equation 30, the voltage across the capacitor 3 are represented as:

\[
V_{c3}^* = \frac{nD}{D_L} V_{in}^* 
\]  
(31)

Same like, equation 19, 25 and 28 are substituting into 29, 22 and 27, 28 into 30 the capacitor of 1 and 2 voltage stress are represented as:

\[
V_{c1}^* = \frac{D+D_L}{D_L} V_{in}^* 
\]  
(32)

\[
V_{c2}^* = (n+\frac{nD}{D_L}) V_{in}^* 
\]  
(33)

The equation of 20, 26, 28, 32 and 33 are substituting into 30 the proposed converter gain of the voltage is obtained from discontinuous mode of operation are represented as:

\[
V_o^* = \left[\frac{2D}{D_L}(1+n)+(n+2)\right] V_{in}^* 
\]  
(34)

\[
D_L = \frac{2D (1+n) V_{in}^*}{V_o^* - (2+n) V_{in}^*} 
\]  
(35)

In fig 5, the average current is represented by

\[
i_{co1} = \frac{1}{2} D_L \frac{V_{L1}^{mp}}{2+2n} \cdot I_o^* 
\]  
(36)

The current of the output capacitor 1 is zero for steady state analysis and 21, 35 and i_{co1} is equal to zero’s are substituted in equation 36.

Therefore

\[
\frac{D^2(n+1)^2 V_{in}^*}{V_o^* - (2+n) V_{in}^*} \cdot \frac{V_o^*}{2(2+n) L_m} = \frac{V_o^*}{R} 
\]  
(37)

The magnetic inductance of the time constant is defined as

\[
\tau_L^* = \frac{L_m}{R^2} 
\]  
(38)

<table>
<thead>
<tr>
<th>Name of the Converters</th>
<th>Quantity of Components</th>
<th>(\eta_{max})</th>
<th>(\frac{V_{Input^<em>}}{V_{Output^</em>}})</th>
<th>Gain of the Voltage ((M^{<em>C_{CCM}} = \frac{V_{Input^</em>}}{V_{Output^*}}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Gain Converter</td>
<td>6 Diodes 5 Capacitor</td>
<td>96.4%</td>
<td>(V_{in} = 24 V) (V_o = 410 V)</td>
<td>(M_{CCM}^* = \frac{2(n+2)}{2(n+2)+D_n} + D)</td>
</tr>
<tr>
<td>[6]</td>
<td>3 Diodes 4 Capacitor</td>
<td>-</td>
<td>(V_{in} = 48 V) (V_o = 380 V)</td>
<td>(M_{CCM}^* = \frac{1+D_n}{1+D} + n)</td>
</tr>
<tr>
<td>[8]</td>
<td>4 Capacitor 4 Diodes</td>
<td>95.8%</td>
<td>(V_{in} = 24 V) (V_o = 400 V)</td>
<td>(M_{CCM}^* = \frac{2n+D_n}{2(n+2)} + D)</td>
</tr>
<tr>
<td>[9]</td>
<td>4 Capacitor 4 Diodes</td>
<td>96.7%</td>
<td>(V_{in} = 24 V) (V_o = 400 V)</td>
<td>(M_{CCM}^* = \frac{1+n+D_n}{1+D} + n)</td>
</tr>
<tr>
<td>[19]</td>
<td>5 Capacitor 5 Diodes</td>
<td>95.7%</td>
<td>(V_{in} = 24 V) (V_o = 200 V)</td>
<td>(M_{CCM}^* = \frac{1+D_n}{1+D} + n)</td>
</tr>
<tr>
<td>[22]</td>
<td>3 Capacitor 5 Diodes</td>
<td>96.2%</td>
<td>(V_{in} = 35 V) (V_o = 200 V)</td>
<td>(M_{CCM}^* = \frac{2(n+2)}{2(1+D)} + D)</td>
</tr>
<tr>
<td>[29]</td>
<td>3 Capacitor 5 Diodes</td>
<td>96.5%</td>
<td>(V_{in} = 36.5 V) (V_o = 200 V)</td>
<td>(M_{CCM}^* = \frac{2(n+2)}{(1+D)^2} + D)</td>
</tr>
<tr>
<td>[31]</td>
<td>3 Capacitor 3 Diodes</td>
<td>95.2%</td>
<td>(V_{in} = 24 V) (V_o = 200 V)</td>
<td>(M_{CCM}^* = \frac{2(n+2)}{(1+D)^2} + D)</td>
</tr>
</tbody>
</table>

Table 1. Proposed converter compared with Conventional Converters

**PV Systems based High Gain Converter using CI and SCC Techniques (S.Sankaranant and P.Sivaraman)**
Equation 38 is substituting in equation 37, the voltage gain is obtained as follows

\[
M_{\text{DCM}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2n+2}{2} + \sqrt{\frac{(2n+2)^2}{4} + \frac{D^2(n+1)}{(2n+2)L_m}}
\]

(39)

3.3. The CCM and DCM Boundary Condition

For the higher Gain converters CCM and DCM, the edge-condition mode of power improvement is same. Equation 18 and 39 based time-constant of the L is expressed as

\[
\tau_{\text{Lmb}}^* = \frac{D^2(n+1)}{(2n+2)^2 + (2n+2)^2} \frac{2}{4}
\]

(40)

Boundary condition of Duty cycle and \(\tau_{\text{Lmb}}^*\) is represented in Fig.13. The \(\tau\) is greater than the \(i_{\text{Lmb}}\) the converter operates like CCM otherwise DCM. Table 1 represents the comparison of proposed converter with other conventional converters. The maximum efficiency obtained for the proposed converter is 96.4% which is much higher than the other conventional converters. Table 2 represents the voltage stress comparison with existing methods.

<table>
<thead>
<tr>
<th>Comparison</th>
<th>Switch Drain-Source Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed</td>
<td>Formula</td>
</tr>
<tr>
<td>[13]</td>
<td>(V_o/(1+n))</td>
</tr>
<tr>
<td>[14]</td>
<td>(2V_o/(n+2))</td>
</tr>
<tr>
<td>[15]</td>
<td>(V_o/(n+2))</td>
</tr>
</tbody>
</table>

Table 2. Comparison Table for Voltage Stress

![Graph showing Duty cycle and \(\tau_{\text{Lmb}}^*\)]

Figure 13. The High Gain Converter boundary condition n=3

4. THE DESIGN PROCEDURE OF HIGH GAIN CONVERTER

The recital of projected converter at 150 W to be tested and measured. The specification of projected converter is as mentioned below and verify the performance of the proposed converter, a prototype of the basic structure circuit is implemented in the laboratory.

- \(V_{\text{in}}^*\) – Input-direct current voltage: 24V
- \(V_{\text{out}}^*\) – Output-direct current voltage: 410V
- \(P_{\text{max}}^*\) – Extreme production power: 150W
- \(F_s^*\) – Switch frequency: 50 KHZ
- S – Switch: IXTH130N10T1
- D – diodes-D1, D2 and D3: DSEI-30-10A; Dinput and D4: 25JPE401
- C- capacitors-C1*: 100 \(\mu F\)/100 Volt, C2: 100 \(\mu F\)/250 Volt, C3: 100 \(\mu F\)/100 Volt, and C01: 220 \(\mu F\)/400 Volt aluminium- capacitors
- T- Transformer- ETDI-49 core PC*: 32, Np*: Ns* = 1:3, Lm*: 32 \(\mu H\) and Lk*: 0.22 \(\mu H\); k = 0.993.

The subordinate current and \(I_{\text{Lk}}^*\) \(V_{\text{DS}}\) of the primary switch under full load condition \(P_o^*\) = 150W, input voltage is 24 V is represented in Fig. 14 (a). The incessant conduction mode of process when the switch is at condition ON, no current flowsthrough the proposed circuit. Coupled-inductor’s subordinate power waveform is represented in Fig 14 (b).
The $I_{c1}$ is transferred to the diode 2, and the amount of energy is transferred to output capacitor 2 when switch "S" is in ON condition. When switch "S" is turned off, energy is absorbed in capacitor C1 from the input voltage and the parasitic capacitor. For the diode and for charging the capacitor, the voltage is absorbed from the input voltage and subordinate-side of the coupled-inductor waveforms as represented in Fig. 14 (c). The diode’s input and output current waveforms are illustrated in Fig. 14 (d). The input voltage energy, though an input to the capacitor, is delivered to the stepper-up circuitry and is transferred to the D output. The output voltage capacitor 1,2, and 3 is represented in fig. 15 (a). It satisfies the equations 14,15, and 17. The $CV_{in}$ and $CV_{out}$ are represented in fig. 15 (b). The proposed converter efficiency at 150 W loads and max is 96.4%, as represented in fig 16. The output voltage waveform obtained from the prototype is illustrated in fig 18. Load step change occurred during simulation is illustrated in Fig 19. Fig 20 and 21 depicts the leakage inductor current and diode output current obtained from the proposed model.

Figure 14. Full Load Condition experimental waveform output power $P_o^* = 150$W
Figure 15 (a). Full Load Condition experimental output voltage capacitor

Figure 15 (b). Full Load Condition experimental CV_{in} and CV_{out} waveform output power P_o^* = 150W.

The experimental prototype of proposed converter is shown in Fig. 17.

Figure 16. The proposed converter efficiency at 150W loads

Figure 17. Experimental 150 W prototype in laboratory
PV Systems based High Gain Converter using CI and SCC Techniques (S.Sankaranant and P.Sivaraman)
5. CONCLUSIONS

The converter was successfully integrated using high gain step-up circuits and coupled-inductor. The capacitor charged and discharged based on high-voltage gain was successfully achieved. Without a high duty cycle, a high stepper-volt gain is achieved by using a coupled-inductor and a capacitor. Clamp circuitry is utilised to resolve energy loss from outflow inductance and minimise switch voltage spike problems. The switching loss was reduced by using fewer voltage-stress components and a minimum conducting resistance Rds. The proposed converter prototype was constructed with Vin 24V into 410V and Pmax = 150W to get a maximum efficiency of almost 96.4% and minimise the switching losses.

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