Indonesian Journal of Electrical Engineering and Informatics (IJEEI)
Vol. 6, No. 4, December 2018, pp. 471~476
ISSN: 2089-3272, DOI: 10.11591/ijeei.v6i1.816

Design and Analysis of High Gain Low Power CMOS Comparator

Labonnah Farzana Rahman[1], Mamun Bin Ibne Reaz[2], Wan Irma Idayu Restu[3], Mohammad Marufuzzaman[4], Lariyah Mohd Sidek[5]
[1,2,3]Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Malaysia
[4,5]Sustainable Technology and Environment Group, Universiti Tenaga Nasional, Malaysia

Article Info

Article history:

Received Nov 8, 2018
Revised Nov 27, 2018
Accepted Dec 19, 2018

Keyword:

CMOS
comparator
high gain
low power
two-stage

ABSTRACT

The comparator is the most significant component of the analog-to-digital converter, voltage regulator, switching circuits, communication blocks etc. Depending on the various design schemes, comparator performance varied upon target applications. At present, low power, high gain, area efficient and high-speed comparator designed methods are necessary for complementary metal oxide semiconductor (CMOS) industry. In this research, a low power and high gain CMOS comparator are presented which utilized two-stage differential input stages with replication of DC current source to achieve higher gain, higher phase margin, higher bandwidth, and lower power consumption. The simulated results showed that, by using a minimum power supply of 1.2 V, the comparator could generate higher gain 77.45 dB with a phase margin of 60.08°. Moreover, the modified design consumed only 2.84 µW of power with a gain bandwidth of 30.975 MHz. In addition, the chip layout area of the modified comparator is found only 0.0033 mm^2.

Corresponding Author:

Labonnah Farzana Rahman
Department of Electrical, Electronic and Systems Engineering,
Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia,
43600 Bangi, Selangor, Malaysia.
Email: labonnah.deep@gmail.com

1. INTRODUCTION

The comparator is the key building block in the design process of ADC, which controls the performance and the accuracy of ADCs. Switching power regulators, data receivers, memory circuits, radio frequency identification (RFID), etc. requires high-speed, high gain and low-power comparators. Therefore, high-performance comparators are necessary to amplify small input voltage to a big output voltage. Consequently, a faster and accuracy based comparator involves high gain and high bandwidth [1]. A comparator is a main building block in voltage regulator process, which controls the output and accuracy of the voltage regulator. High-speed, high-resolution, small power with the reduced area are several requirements in devices such as switched-mode power supplies, ADC, data transmission circuit, voltage reference, and etc. [2]-[6]. A new design of comparator with a lower power supply voltage is developed to fulfill the features stated, where a suitable topology is chosen to design the operational amplifier.

The operational amplifier as a comparator is a circuit that produces one output, which depends on the comparison of the reference voltage and analog signal. In an epitome comparator, the gain obtained is infinite with zero volts of the offset voltage. However, a finite gain is obtained in practical application [7]. Main features of high speed, medium to high gain and stability with large loads are found in single-stage amplifiers. However, reduction of power supply voltage and intrinsic gain of transistor often traded for gain and output swing in single-stage amplifiers [8]. Several topologies have been introduced to improve gain and output swing in a single-stage amplifier such as a two-stage, folded cascade and telescopic [9]-[11]. A two-

stage amplifier is often implemented to achieve higher gain as it provides higher output swing in the second stage [9]. It also provides better CMRR, lower power consumption and slew rate [8], [12]. However, it requires frequency compensation for stability in closed loop application where this amplifier has multiple zeros and poles [8], [11], [12]. Folded cascade amplifier has an advantage in providing a better power supply rejection ratio (PSRR), high speed and extensive frequency response. However, the gain and output swing is lower compared to two-stage topology. It also consumes more power and reduced common mode rejection ratio (CMRR) and slew rate [9]-[11]. Telescopic topology provides a high-speed operation and lowers power consumption and noise compared to the other two topologies. However, telescopic topology has an equal performance in output swing and gain with folded cascade topology but still lesser than two-stage topology [9]-[11].

In this research, a modified comparator is presented, which is based on two-stage differential amplifier input stages. Moreover, this modified design has a level shifting stage, which is capable of providing higher gain with lower power consumption and lower power supply compared to other topologies based on the simulation result.

2. INTRODUCTION

The design consideration of the comparator includes gain, offset voltage, phase margin, slew rate, settling time and power dissipation [13]. Therefore, to design a comparator circuit a two-stage op-amp circuit is chosen to get the desired outputs. The modified design of the comparator is implemented based on the two-stage operational amplifier. From Figure 1 it is shown that, this comparator circuit consists of a DC current source, which is replaced with two transistors to replicate a constant current source.

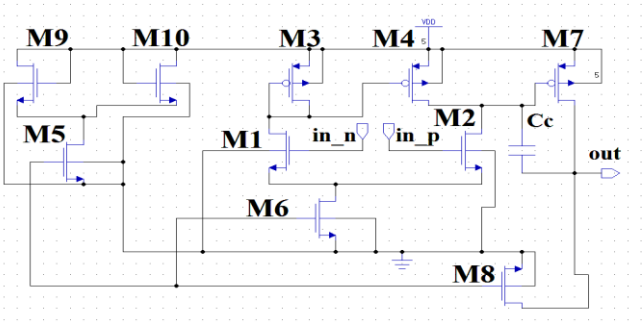


Figure 1. Schematic diagram of the comparator circuit

The modified design has three stages, current source, two-input differential mode amplifier and common source amplifier. In the first stage, a DC current source is utilized, which consists of two NMOS transistor to work as the biasing circuit. On the other hand, the second stage consists of a two-input differential mode amplifier with single-ended output, which can provide higher gain, CMRR, PSRR, slew rate and lower power consumption. Moreover, this stage also converts the differential input voltage to the current output, which is subsequently applied to a current mirror load. The last stage consists of common source amplifier to perform level shifting, gain boosting, and current to voltage conversion with the single output voltage. Since the signal feedback into the closed-loop application, level shifting is used to compensate any changes in dc voltage in input stages. It is also used to achieve a higher phase margin so that the system achieved stability. To obtain a high gain and high bandwidth, the phase margin is often traded. Since there is a capacitor connected between the input and output of the last stage, the pole is used to split, and the phase margin is improved without reducing output gain. In addition, less variation is shown in the desired output signal [14]. Generally, the output of a differential comparator is proportional to the difference between the two voltages as shown (1)

$$V_{out} = A(V_{in}^{+} - V_{in}^{-}) \quad (1)$$

where, A is the gain of the comparator, which is again defined by the (2),

$$V_{Gain} = 20 \log \frac{V_{out}}{V_{in}} \quad (2)$$

On the other hand, the common-mode rejection ratio (CMRR) is the ratio between two differential-mode gain and common-mode gain, specify the capability of the comparator to cancel voltages that are common for both input voltages. The CMRR is defined as (3),

$$CMRR = 20 \log 10 \frac{A_d}{|A_c|} \quad (3)$$

where A_c is the common-mode gain of the comparator.

The chip layout of the proposed comparator circuit is shown in Figure 2, where the chip layout occupies a small area of 57.9 µm x 57.5 µm. During the design process, all transistors and capacitors are placed in a manner that reduces the mismatch and parasitic capacitance.

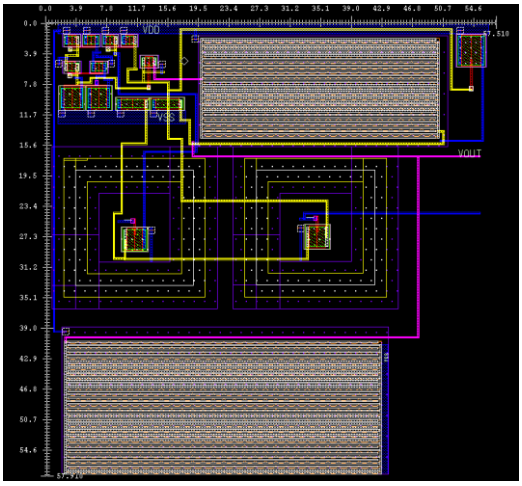


Figure 2. Die layout of the comparator without pads

3. RESULTS AND ANALYSIS

The comparator circuit is simulated using ELDOSPICE simulator (Mentor Graphics) in Silterra 0.13 µm CMOS process. Several analyses conducted to observe the behavior of the modified comparator circuit. One of the analyses is a transient response, which shown in Figure 3. A positive sine wave is applied at positive input (V+) and negative sine wave was applied at the negative input (V-) of the comparator. The output from comparator reaches almost the same value as VDD when the difference between V+ and V- is bigger than V+. On the other hand, when the difference between V+ and V- is smaller than V+, the output of the comparator is 0V. This result validates the theory of the comparator successfully.

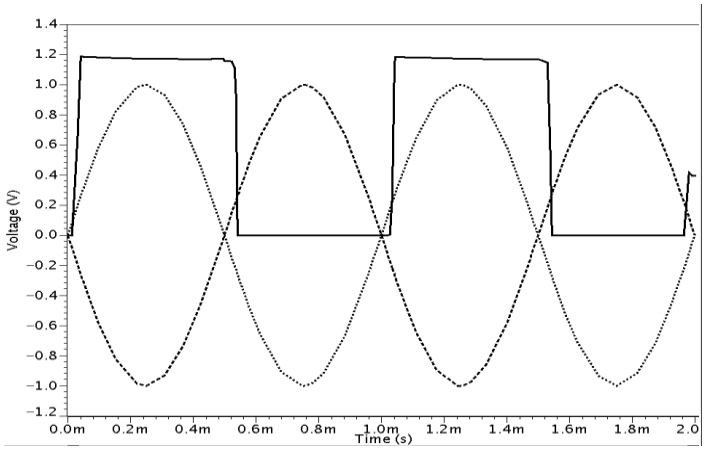


Figure 3. Transient simulation of the comparator circuit

In this research, the improved design can produce a higher output with lower input. Therefore, a higher gain is needed to complete the desired specification. In Figure 4, the simulated results show that the modified circuit can produce a gain of 77.45 dB. Since the phase margin is often traded with a higher gain, therefore, in this research the designed comparator circuit can maintain the phase margin at 60.08°, which is the typical value for a comparator to operate in a stable condition. In addition, the gain bandwidth is also maintained as 30.975 MHz, which refers to unity gain or gain bandwidth product (GBP). This GBP can be defined by the (4):

$$GBP = Gain \times Bandwidth = A \times BW \quad (4)$$

By using the above-mentioned equation, if the frequency is 2.9 kHz, where the gain is 77.45 dB, then the GBP is found 21.70 M. Similarly, if the frequency is 30.97 MHz, where the gain is -3 dB, the GBP is also found as 21.70 M. Therefore, it is clear from this research that, the proposed comparator is well functioning within the desired bandwidth ranges with a unity gain.

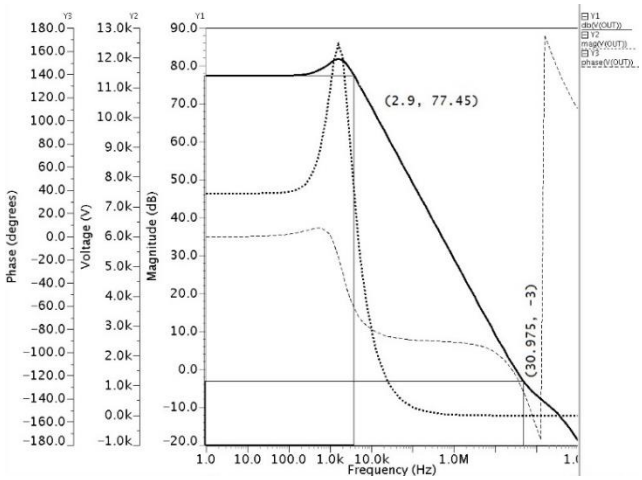
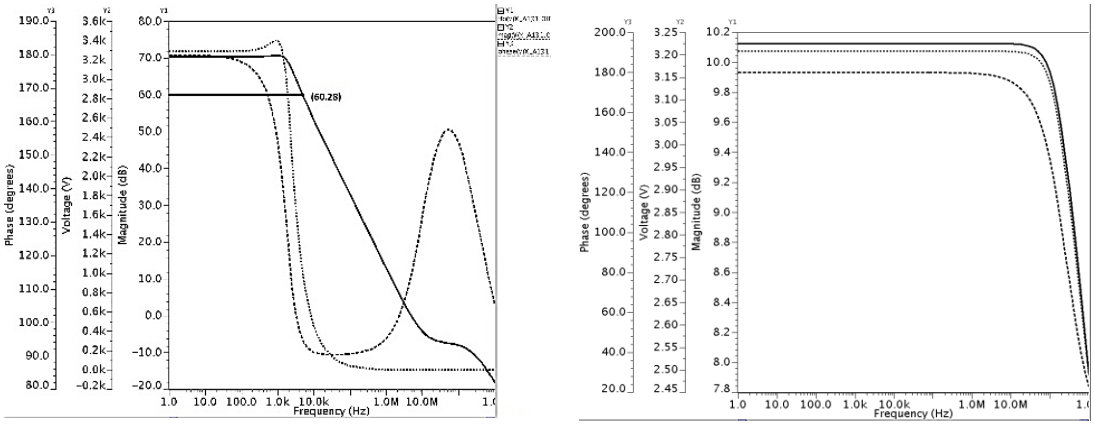


Figure 4. AC Analysis of the proposed comparator circuit

The CMMR analysis is illustrated in Figure 5 (a) and (b). The idea is to show the capability of the input to reject input signals common to both input terminal. Since the expression of gains in logarithmic units of dB, differential mode gain subtracts the common mode gain, which results of 60.28 dB. Finally, a comparison work is tabulated among various techniques for designing the comparator, which is shown in Table 1.



(a) (b)

Figure 5. Gain analyses for (a) differential and (b) common-mode

From Figure 6 it is shown that this comparator circuit achieved lower power dissipation, which is only 2.84 µW under supply voltage 1.2 V. In this research works, the lower power dissipation is obtained by maintaing the proper transistor sizing and small capacitnace values, which helps to dissipates lower power than [12].

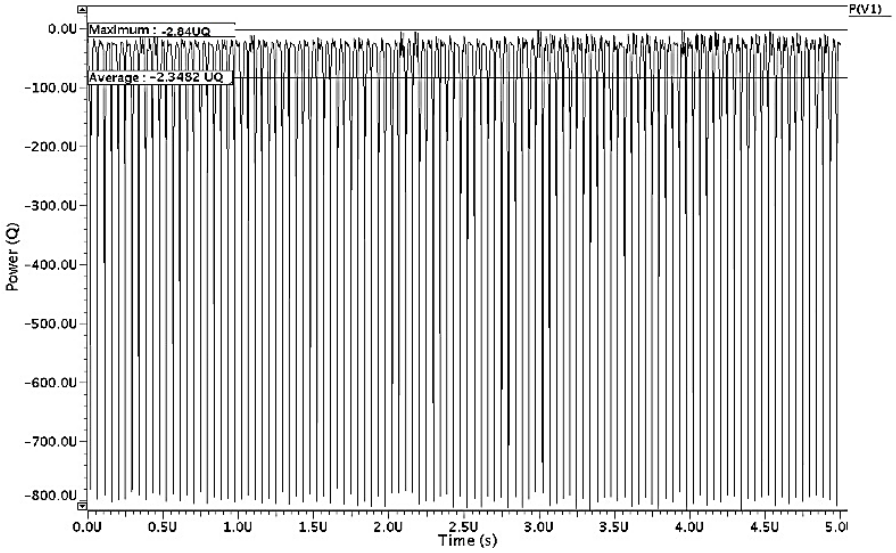


Figure 6. Simulated waveform of power dissipation of the proposed comparator

Table 1 Performance comparison of different comparator circuits

Parameters	[13]	[15]	[16]	[17]	This work
Technology (um-CMOS)	0.13	0.18	0.13	0.18	0.13
Supply voltage (V)	1.8	3.3	1.2	1.8	1.2
Output gain (dB)	69.73	92.27	65	60	77.45
Phase Margin (°)	60.25	-	81.08	79	60.08
Gain Bandwidth (MHz)	28.4	136.8	71.39	170	30.975
CMRR (dB)	62.93	-		49	60.28
Power dissipation (µW)	389	-		-	2.84
Chip Area (mm^2)	2.44	0.00532		-	0.0033

From Table 1, it is shown that the output gain and gain bandwidth of this research is found lower compared to [15]. However, the supply voltage of [15] is found 3.3V while in this research the designed comparator circuit used only 1.2 V as the supply voltage. Although the supply voltage is only 1.2 V, the output gain produced by this research is more than 60 dB, which satisfy the overall design specifications. Above all, the comparator circuit consumed only 2.84 µW power, which is found better compared to [13]. By using only ten transistors scheme with only one capacitor the modified circuit can significantly reduce the power dissipation. Moreover, in a DC analysis, the comparator showed that the improvement in power dissipation is found only 0.111 mW. Moreover, the chip layout area of this designed comparator is found only 0.0033 mm^2, which is also lower compared to other research works. In this research, two NMOS transistors worked as the biasing circuit whereas two-input differential mode amplifiers with single-ended output were used, which helped to reduce the power dissipation as well as produced enough gain.

4. Conclusion

A modified design of the comparator circuit with high-gain, low power and low chip layout area is presented in this research works. The design used only ten transistors with only one capacitor which helps the circuit to reduce the overall power dissipation of only 2.84 µW. Moreover, two NMOS transistor is used as the biasing circuitry to help to reduce the power consumption. The results clearly reveal that, the improved comparator is able to function properly with a higher gain 77.45 dB with a phase margin of 60.08°and lower chip layout area of only 0.0033 mm^2. In addition, the simulation result shows an acceptable CMRR and ICMR with a high gain bandwidth of 30.975 MHz.

REFERENCES

[1]. Rahman L.F., Reaz M.B.I., Yin C.C., Ali, M.A.M., and Marufuzzaman M., "Design of high speed and low offset dynamic latch comparator in 0.18 µm CMOS process," *PloS one*, 2014, vol. 9(10).

[2]. Milovanović V., and Zimmerman, H., "A fully differential CMOS self-biased two-stage preamplifier-latch threshold detection comparator," *Proceedings of the 2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, Beijing, China, pp. 606 – 609, May 2013.

[3]. Gandhi P.P., and Devashrayee N.M., "High-performance CMOS voltage comparator," *Proceedings of the Nirma University International Conference on Engineering (NuiCONE)*, Ahmedabad, India, pp. 1-5, Nov 2013.

[4]. Vanitha R., and Thenmozhi S., "Low power CMOS comparator using bipolar CMOS technology for signal processing applications," *Proceedings of the International Conference on Electronics and Communication System (ICECS)*, Coimbatore, India, pp. 1241-1243, Feb 2015.

[5]. Yang B.D., "250-mV supply subthreshold CMOS voltage reference using a low-voltage comparator and a charge-pump circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61(11), pp. 850-854, 2014.

[6]. Rahman L. F., Reaz M. B. I., Marufuzzaman M., Mashur M. B., & Badal M. T. I., "Evaluation of Low Power and High-Speed CMOS Current Comparators," *Transactions on Electrical and Electronic Materials*, vol. 17(6), pp. 317-328, 2016.

[7]. Yadav A., "Design of two-stage CMOS Op-Amp and analyze the effect of scaling," *International Journal of Engineering Research and Applications (IJERA)*, vol. *2*(5), pp. 647-654, 2012.

[8]. Mesri A., Pirbazari M.M., Hadidi K., and Khoei A., "High gain two-stage amplifier with positive capacitive feedback compensation," *IET Circuits, Devices & Systems*, vol. 9(3), pp. 181-190, 2015.

[9]. Baharudin S.N.S., Jambek A.B., and Ismail R.C., "Design and analysis of a two-stage OTA for sensor interface circuit," *Proceedings of the IEEE Symposium on Computer Applications & Industrial Electronics*, Penang, Malaysia, pp. 88-92, Apr 2014.

[10]. Hamzah M.H., Jambek A.B., and Hashim U., "Design and analysis of a two-stage CMOS op-amp using Silterra's 0.13 µm technology," *Proceedings of the 2014 IEEE Symposium on Computer Applications and Industrial Electronics (ISCAIE)*, Penang, Malaysia, vol. 55-59, Apr 2014.

[11]. Yadav A., "A Review Paper on Design and Synthesis of Two stage CMOS OP-Amp," *International Journal of Advances in Engineering & Technology*, vol. 2(1), pp. 677, 2012.

[12]. Raut K.J., Kshirsagar R.V., and Bhagali A.C., "A 180 nm low power CMOS operational amplifier," *Proceedings of the 2014 Innovative Applications of Computational Intelligence on Power, Energy and Controls with their impact on Humanity (CIPECH)*, Ghaziabad, India, pp. 341-34, Nov 2014.

[13]. Idris M.I., Yusop N., Chachuli S.A.M., Ismail M.M., Arith F., and Darsono A.M., "Low Power Operational Amplifier in 0.13 um Technology," *Modern Applied Science*, vol. 9(1), pp. 34, 2014.

[14]. Patel V.J., and Patel M.L., "Low Power Wide Frequency Range Current Starved CMOS VCO in 180nm, 130nm and 90nm CMOS Technology," *International Journal of Engineering Research and Development*, vol. *7*(4), 2013.

[15]. Mahalingam S., Mamun M., Rahman L., and Zaki W.M.D.W., "Design and analysis of a two-stage operational amplifier for high gain and high bandwidth," *Australian Journal of Basic and Applied Sciences*, vol. *6*(7), pp. 247-254, 2012.

[16]. Shivani M.; and Gupta P., "An Extremely Low Power Consumption Operational Amplifier with High Phase Margin and Gain in 130 nm Technology," *International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE)*, vol. 2(11), pp. 875-879, 2013.

[17]. Sharma K., "170 MHz GBW, two-stage CMOS operational amplifier with high slew rate using 180 nm technology," *Proceedings of the Annual IEEE India Conference (INDICON)*, New Delhi, India, pp. 1-5, 2015.