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Effect of clock gating in conditional pulse enhancement flip-flop for low power applications

Kuruvilla John[1], Vinod Kumar R. S.[2], Kumar S. S.[3]
[1,2]Department of Electronics and Communication Engineering, Noorul Islam Centre for Higher Education, India
[3]Department of Electronics and Instrumentation Engineering, Noorul Islam Centre for Higher Education, India

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ABSTRACT

Flip-Flops (FFs) play a fundamental role in digital designs. A clock system consumes above 25% of total system power. The use of pulse-triggered flip-flops (P-FFs) in digital design provides better performance than conventional flip-flop designs. This paper presents the design of a new power-efficient implicit pulse-triggered flip-flop suitable for low power applications. This flip-flop architecture is embedded with two key features. Firstly, the enhancement in width and height of triggering pulses during specific conditions gives a solution for the longest discharging path problem in existing P-FFs. Secondly, the clock gating concept reduces unwanted switching activities at sleep/idle mode of operation and thereby reducing dynamic power consumption. The post-layout simulation results in cadence software based on CMOS 90-nm technology shows that the proposed design features less power dissipation and better power delay performance (PDP) when compared with conventional P-FFs. Its maximum power saving against conventional designs is up to 30.65%.

Corresponding Author:

Kuruvilla John,
Research Scholar, Department of Electronics and Communication Engineering,
Noorul Islam Centre for Higher Education,
Thucklay, Tamilnadu, India, 629180.
Email: kuruvilla08@gmail.com

1. INTRODUCTION

In all kinds of digital structures flip-flops are widely used as the basic storage element. It is also estimated that above 25% of the total system power is consumed by the clock system [1]. Thus, FFs contributes a major part of the power consumption of the total system. P-FF exhibits better performance than conventional master-slave FF designs in low power and high-speed applications [2]. The single latch structure design of P-FFs made them more popular than conventional master-slave and transmission gate-based FF designs in low power and high-speed applications [3].

The generator and latches are the basic parts in the structure of a P-FF design are pulse. The trigger pulses are generated by the pulse generator which may be generated either at any edges of clock signals or at both edges of clock signals. The latch structure performs the latching or sampling of the input data into the output based on the generation triggering pulses. Depending upon the pulse generation mechanism, P-FFs are classified as a single and double edge triggered types [4].

Based on the connection of pulse generation logic and latch, P-FFs are classified as implicit and explicit types [5]. In implicit case, the pulse generator is inbuilt in the latch structure and in explicit it is external to the latch structure. It is estimated that due to the control of discharging path the implicit P-FFs are more power efficient than explicit types [6-8]. However, the sharing of pulse generator among neighboring latches is an advantage of explicit P-FF. Both implicit and explicit P-FFs face the longest discharging path problem in the latch structure. This increases the size of the transistors used at the pulse generator to enlarge the width and height of triggering pulses for the sufficient capturing of data.

An unnecessary switching activity in a P-FF causes a lot of wastage in power consumption. Using various techniques such as conditional discharging [9], conditional data mapping [10], conditional capturing [11], signal feed-through [12-13], power gating [14], error masking [15] and clock gating [16-18], unwanted switching activities can be avoided and thus the power consumption can be reduced.

In this paper, a low power P-FF is presented which has an implicit style of operation. This structure solves the longest discharging path problem in the latch and unwanted switching activities at sleep/idle mode of operation. The remaining part of the paper is organized as follows: Section 2 describes two conventional P-FF designs, which includes single-ended conditional capturing energy recovery FF (SCCERFF), and conditional pulse enhancement FF (CPEFF). Section 3 explains the proposed low power P-FF design. Section 4 compares the P-FFs and presents the results after simulation. The paper concluded in section 5.

2. CONVENTIONAL DESIGNS

This section explains the operation of two implicit P-FFs namely (i) Single Ended Conditional Capturing Energy Recovery FF (SCCERFF), and (ii) Conditional Pulse Enhancement FF (CPEFF).

2.1. Single ended conditional capturing energy recovery flip-flop

The Single ended conditional capturing energy recovery (SCCER) FF is a refined P-FF design for low power applications [19]. The circuit diagram of SCCERFF is shown in Figure 1. The energy recovery technique is used to improve the power efficiency of digital circuits. Energy recovery technique improves the energy efficiency by preventing the flow of current through low voltage drop devices and energy stored on their capacitors is recycled. The consumption of power in the clock network can be reduced by an innovative technique known as conditional capturing. The pulse generation logic consists of inverter I1 and transistors N1 and N2. The trigger pulses are generated at node Y. The load capacitance at node X can be reduced using an always ON pMOS transistor P1 in combination with an inverter I3. The undesired transition activities at node X can be avoided by using an additional nMOS transistor N3 gated by Q_fdbk.

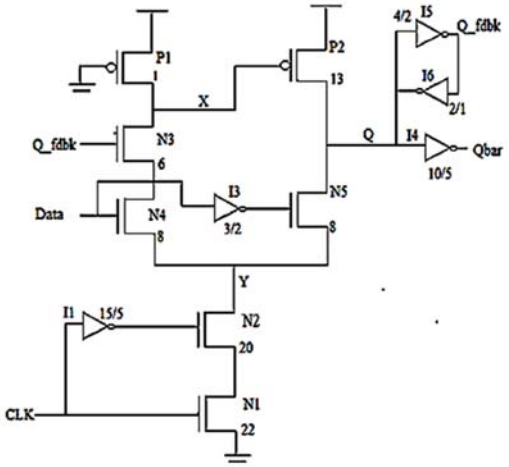

Figure 1. Circuit diagram of SCCERFF

2.2. Conditional pulse enhancement flip-flop

The circuit diagram of conditional pulse enhancement flip-flop (CPEFF) [20] is shown in Figure 2. In CPEFF a two-input AND gate of N-type pass-transistor logic (PTL) style is formed by the transistors N2 and N3. The N-type PTL transmits only weak ones (VDD-Vtn) to the output. At node Z the value of pulse signal is zero in most of the time other than transition edges of clock signals, because of the two complementary inputs of the AND gate. The node Z reaches a temporary floating state when the clock signal falls to the LOW value. Both transistors N2 and N3 are turned ON at the rising edges of the clock signal. This passes a weak logic high value (VDD-Vtn) to node Z, which causes turning ON of transistor N1 by a time period inserted by the delay of inverter I1. The enhancement in the width and height of the triggering pulse takes place by an additional pMOS transistor P3 when the input data changes from 0 to 1 value [21].

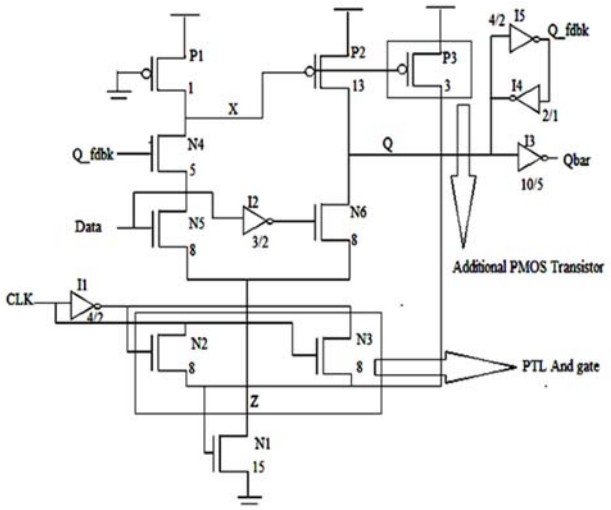

Figure 2. Circuit diagram of CPEFF

The CPEFF is having better performance in power, speed and area than conventional P-FF. This P-FF solves the pulse width control issue but unwanted switching activities take place during sleep/idle mode of operation, which will increase the power consumption and degrade the total performance.

3. PROPOSED DESIGN

Clock gated conditional pulse enhancement flip-flop (CGCPEFF) is specially designed for low power applications. The application of clock gating technique [22-24], which aims in the further reduction of clock power in sleep/idle mode of operation is proposed here. The proposed P-FF solves the longest discharging path problem of latch structure and unwanted switching activities at sleep/idle mode of operation. This design has all the features of CPEFF with an additional NOR gate for enabling the clock gating concept into it.

The power exerted by the logic gates in connection with the clock and the power of the remaining part of the flip-flop circuit are the two components of power dissipation inside flip-flops. A flip-flop mainly functions in the active and sleep/idle mode of operation. It is estimated that during the active mode clock must be working and all the switching activities must be at this mode and during sleep/idle mode the clock must be inactive and there will be no switching activities. But unfortunately, the active operations of the clock during sleep/idle mode causes unwanted switching activities and this will increase the power consumption.

In this design, there is a separation in the power exerted by the clock circuit and a remaining circuit. The power consumption of both the clock and the remaining circuit in sleep/idle mode can be reduced by disabling the clock circuit. The proposed clock gating technique can be implemented by disabling the inverter gates present in the pulse generation logic of the conventional P-FF. This can be achieved by replacing the inverter I1 present in CPEFF with a NOR gate as shown in Figure 3 and the complete circuit diagram of the proposed P-FF is in Figure 4.

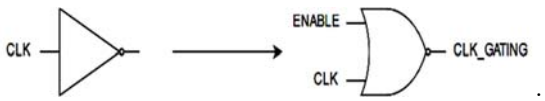

Figure 3. Clock gating concept

In CGCPEFF, a two-input AND gate of N-type pass-transistor logic (PTL) style is formed by the transistors N2 and N3. An additional pMOS transistor P3 is used for enhancing the width and height of triggering pulses when the input data changes from 0 to 1 value. The CLK and ENABLE are the two input signals of the NOR gate. In the active mode, NOR gate behaves like an inverter due to its LOW ENABLE input and the flip-flop operate in the normal fashion. All switching activities take place at this mode of

operation. In the sleep/idle state, the internal clock is disabled by setting the output of the NOR gate to zero due to its HIGH ENABLE input signal. The nMOS transistor N1 present in the pull-down path gets turned off and prevents any data evaluation. This results in saving of clock power by disabling the internal clock. The use of smaller transistors in the NOR gate and also reduced short-circuit power dissipation on the logic gates associated with the clock are the two features of clock gating. Thus the clock gating circuit does not bring in any power overhead in the total system. The larger stack of transistors in the NOR gate reduces its short circuit power when compared with NOT gate.

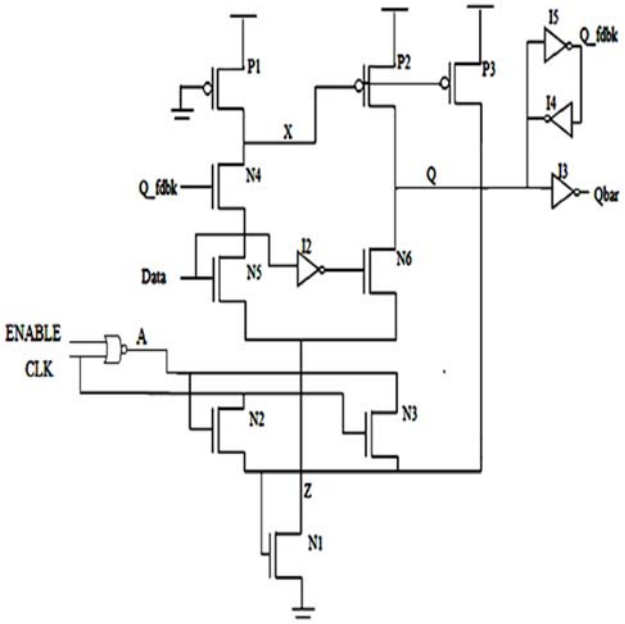

Figure 4. Circuit diagram of CGCPEFF

The discharging of internal node X through the three nMOS transistors N4, N5, and N1 when both input data and inverted output Qbar are HIGH causes the turning ON of pMOS transistors P2 and P3. This will increase the value of trigger pulse at node Z from weak one (VDD-Vtn) to strong one (VDD). The turning OFF of the discharging path occurs after the rising edge of the clock signal, due to the delay of inverter I1 drives the value of triggering pulse at node Z reverse to zero through nMOS transistor N3.

The total power consumption is the combination of dynamic, static and short circuit powers and is given in (1) [25-26].

$$P = P_{dynamic} + P_{static} + P_{short-circuit} \quad (1)$$

In (1), $P_{dynamic}$ is the dynamic power consumption, also known as switching power. Dynamic power depends on several factors, including the frequency of operation (f), square of the supply voltage (V^2), data switching activity (α) and clock load capacitance (CL) as shown in (2).

$$i.e., P_{dynamic} = \alpha C_L V^2 f \quad (2)$$

In CGCPEFF, the clock is inactive during the sleep/idle mode of operation and this will reduce unwanted switching activities. The reduction of unwanted switching activities leads to dynamic power saving. Thus, the embedding of the clock gating concept and conditional pulse enhancement scheme makes the proposed CGCPEFF more power efficient than conventional P-FFs. The clock gating concept is introduced into the flip-flop by replacing inverter present in the clock path with NOR gate, hence is the proposed technique not applicable to flip-flops that do not have an inverter in the clock path.

4. RESULTS AND DISCUSSION

The post layout simulations of all P-FF are done in cadence by using CMOS 90nm technology. The operating condition used in the simulation is 500 MHz/1.5V and temperature of 298K. Figure 5 shows the principle of the clock gating concept. The CLK and ENABLE are the two inputs signals of NOR gate. In the active mode, the ENABLE signal is low, therefore NOR gate behaves like an inverter and inverted version of clock input is obtained at the output. In the sleep/idle state, enable signal is high which inactivates the internal clock by setting the output of the NOR gate to zero. This results in saving of clock power by disabling the internal clock.

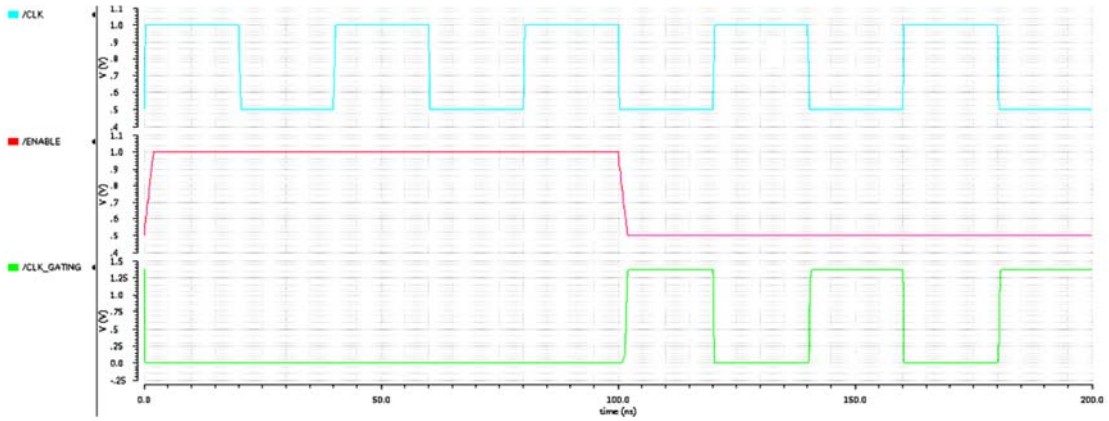

Figure 5. Clock gating concept

The simulation waveform of CGCPEFF is shown in Figure 6. The input data changes are reflected at the output during the rising edges of clock signal hence it is a single edge triggered FF design. Conditional pulse enhancement of the proposed P-FF is shown in Figure 7. When output Q makes a transition from 0 to 1 value, then the width and height of trigger pulses increase from 2.4nS to 2.92nS and 970mV to 1.25V respectively. It is evident from the experimental results, that the pulse width and height is enhanced upon 17.80% and 22.4% respectively when compared with usual operation because of the extra voltage from transistor P3.

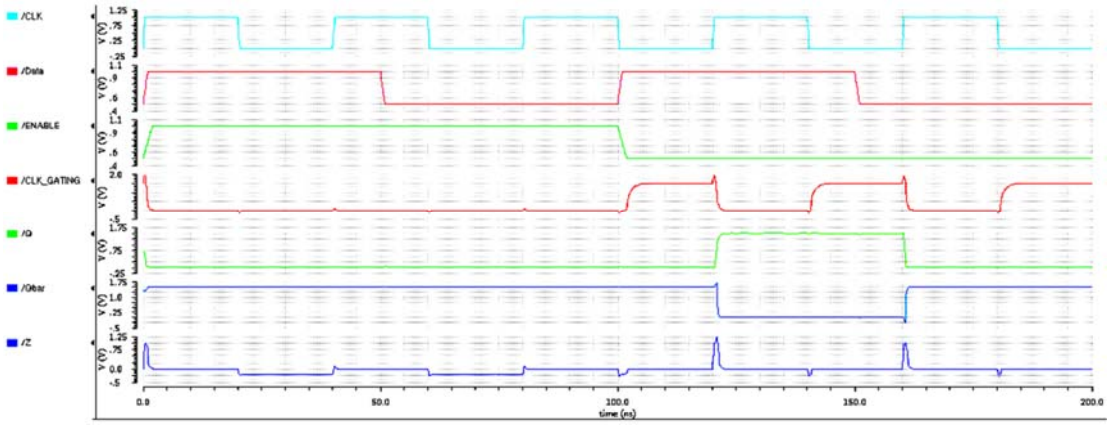

Figure 6. Simulation waveform of CGCPEFF

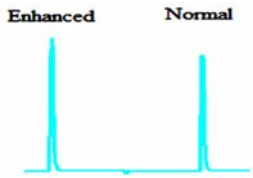

Figure 7. Conditional pulse enhancement in CGCPEFF

From the simulation waveform of proposed P-FF, it is clear that the clock gating divides the flip-flop operation into active and sleep/idle mode. When the ENABLE signal is HIGH, no CLK_GATING signal is formed and as a result, there are no transitions at the output node Q. At this time flip-flop is in sleep/idle mode and simulation results gives the average power consumption at this mode is 930.4nW. During LOW ENABLE the CLK_GATING signal is formed as the inverted value of the clock signal and input data is sampled to the output Q at rising edges of the clock signal. Now the flip-flop is in active mode and average power consumption at this mode is 71.57µW. The embedding of the power reduction techniques in the proposed CGCPEFF reduces the average power consumption to 58.36µW and is shown in Figure 8. Thus the introduction of the clock gating concept in CPEFF makes 18.45% advantage in power saving. Figure 9 shows the layout of the proposed CGCPEFF. A total layout area of CGCPEFF is 335.87µm^2.

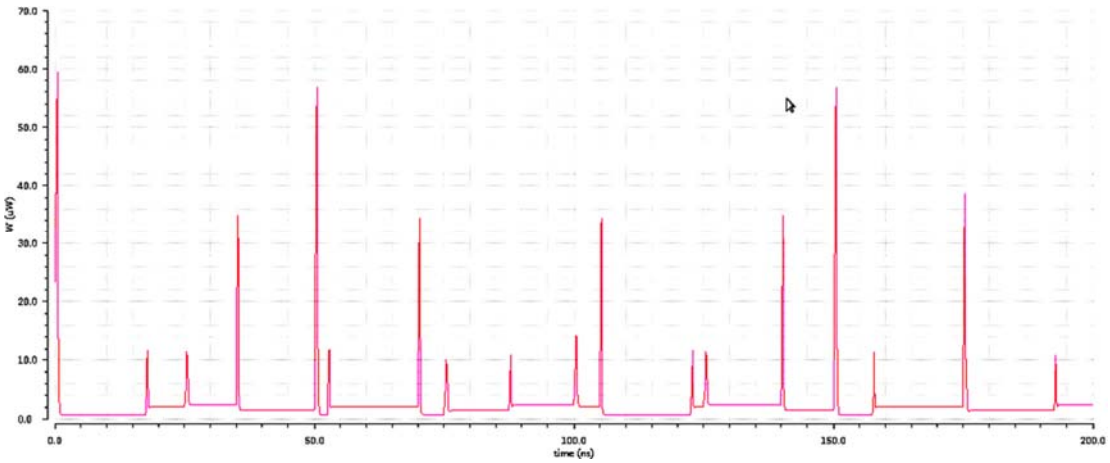

Figure 8. Power consumption of CGCPEFF

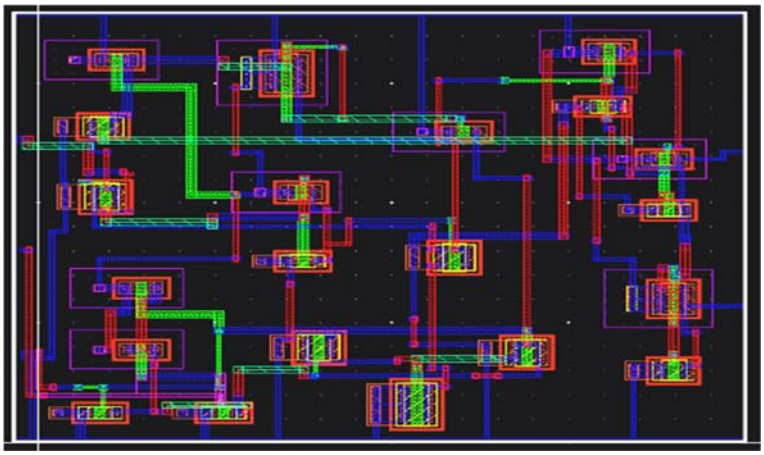

Figure 9. Layout of CGCPEFF

Table 1 summarizes the important performance indexes of proposed CGCPEFF with other conventional P-FF designs. These include transistor count, average power consumption, minimum Data to Q delay, minimum CLK to Q delay, setup time, hold time, power-delay product performance and the layout area. From the simulation result it is clear that the power consumption and power-delay-product (PDP) performance of proposed CGCPEFF outperforms SCCERFF and CPEFF due to the embedding of conditional pulse enhancement technique and the clock gating concept, with slight overhead in delay and area.

In CGCPEFF the clock is inactive during the sleep/idle mode of operation and this will reduce unwanted switching activities. The reduction in unwanted switching activities leads to dynamic power saving. The conditional pulse enhancement scheme increases the speed of latching of data without increasing the delay of inverters and the width of transistors used at the pulse generator. Figure 10 shows the power comparison of proposed CGCPEFF with SCCERFF, and CPEFF. The power consumption of proposed CGCPEFF outperforms the conventional implicit SCCERFF by a margin of 30.65%. Due to the introduction of the clock gating concept, the proposed P-FF is having a power advantage of 18.46% with Data to Q delay overhead of 5.4% when compared with CPEFF. The proposed design is having a negative setup time. Due to negative setup time, CGCPEFF is having a slightly larger hold time requirement. The replacement of inverter in CPEFF with NOR gate for clock gating concept increases the layout area of proposed P-FF. Among the compared P-FFs, CGCPEFF is having the best power-delay product performance due to its reduced power consumption. Figure 11 shows the power-delay-product comparison of proposed CGCPEFF with conventional P-FFs. Table 2 shows a comparison of leakage power consumption.

Table 1. Observation of design parameters

P-FFs	SCCERFF	CPEFF	CGCPEFF
Number of transistors	17	19	21
Average Power Consumption (µW)	84.16	71.57	58.36
Minimum Data to Q Delay (pS)	370.57	331.24	350.32
Minimum CLK to Q Delay (pS)	159.78	142.83	151.04
Setup Time (pS)	-190.70	-122.60	-129.60
Hold Time (pS)	194.60	262.80	277.90
Power-Delay-Product (fJ)	31.18	23.70	20.44
Layout Area (μm^2)	333.60	326.59	335.87

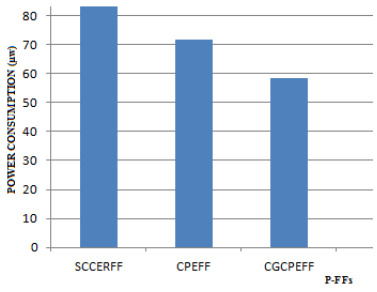

Figure 10. Comparison of power consumption in various P-FFs

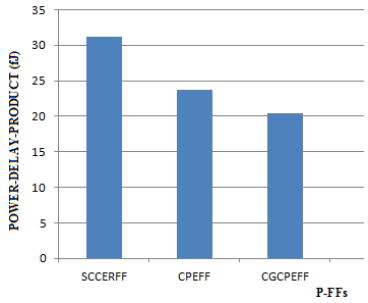

Figure 11. Comparison of power-delay-product in various P-FFs

Table 2. Comparison of leakage power consumption (µW)

P-FFs	SCCERFF	CPEFF	CGCPEFF
(CLK, Data) = (0,0)	1.48	1.01	0.82
(CLK, Data) = (0,1)	1.81	1.10	0.89
(CLK, Data) = (1,0)	1.90	1.33	1.09
(CLK, Data) = (1,1)	2.10	1.43	1.16
Average	1.82	1.21	0.99

5. CONCLUSION

In this paper, we presented a novel P-FF design embedded with conditional pulse enhancement and clock gating concept suitable for low power applications. The enhancement in the width and height of the trigger pulse occurred when output changes from 0 to the 1 value with an extra pMOS transistor in the design. The clock gating concept, which reduces unwanted switching activities at sleep/idle mode by using a NOR

gate-based clock gating signal generation. The longest discharge path problem is solved by the conditional pulse enhancement scheme and the dynamic power consumption is reduced by the clock gating concept. The experimental results show that the proposed P-FF design is having better performance in power and power delay product (PDP) with slight overhead in input to output delay and area.

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BIOGRAPHY OF AUTHORS

Kuruvilla John received his B.Tech and M.Tech degrees in Electronics and Communication Engineering from the Mahatma Gandhi University, Kerala, India, in 2010 and 2014 respectively. He is currently doing his research in Low Power VLSI from Noorul Islam Centre for Higher Education, Tamilnadu, India. He is an Assistant Professor of the Department of Electronics and Communication Engineering, Providence College of Engineering, APJ Abdul Kalam Technological University, Kerala, India. He has more than 5 years of teaching experience and many publications in journals and conferences. His research interest includes Low Power VLSI, VLSI Signal Processing, and Digital Design Principles.

Vinod Kumar. R. S. received his B.E. degree in Electronics and Communication Engineering in 1991 and M.E. degree in Communication Systems in 2000, both from Madurai Kamaraj University, Tamil Nadu, India. He pursued his Ph.D degree from Anna University, Chennai, India, in 2015. His areas of research are VLSI Design, Multiresolution Patch-based Texture Synthesis, Steganography, and Medical Imaging. He has contributed 30 technical papers in various journals, and International/National Conferences. He started his career as Lecturer in Noorul Islam College of Engineering, Tamil Nadu, India in 1993 and presently working as Professor & Head, Department of Electronics & Communication Engineering and Dean, Faculty of Electrical & Electronics Engineering, Noorul Islam Centre for Higher Education, Kumaracoil. He has more than 25 years of teaching experience and thirteen years of research experience. His areas of interest include VLSI, Digital Image Processing, Analog Modulation Systems, Digital Communications, Linear Integrated Circuits, and Digital Electronics. At present, he is guiding 8 Ph.D. scholars. He is a Doctoral Committee member for twelve Ph.D. Part-time/Full-time scholars, in the faculty of Information and Communication Engineering, Anna University, Chennai.

Kumar S. S. received his B.E. degree in Electronics and Instrumentation Engineering from Manonmaniam Sundaranar University, Tirunelveli, India and M.E. degree in Applied Electronics from Anna University, Chennai, India. He pursued his Ph.D. degree from Anna University, Chennai, India. His areas of research are VLSI, Medical Image Processing, Satellite Image Processing, Multiresolution Techniques, and Artificial Intelligence. He has published several technical papers in various journals and conferences. He started his career as Lecturer in Noorul Islam College of Engineering, Tamil Nadu, India in 2005 and presently working as Head, Department of Electronics & Instrumentation Engineering, Noorul Islam Centre for Higher Education, Kumaracoil. He has more than fourteen years of teaching experience and ten years of research experience. He has produced three Ph.D scholars and at present, he is guiding 6 Ph.D. scholars. He is a Doctoral Committee member for ten Ph.D Part-time/Full-time scholars, in the faculty of Information and Communication Engineering, Anna University, Chennai.