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Charge Sharing Suppression in Single Photon Processing Pixel Array

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Abstract

This paper proposes a mechanism for suppression of charge sharing in single photon processing pixel array by introducing additional circuit. The idea of the proposed mechanism is that in each pixel only analog part will introduced, the digital part is shared between each four pixels, this leads to reduce the number of transistors (area). By having communication pixels, a decision that which one of the neighboring pixels shall collect the distributed charges is taken. The functionality, which involves analog and digital behaviors, is modeled in VHDL.

Keywords*: photon, pixel, readout, X-Ray, detector*

1. Introduction

Semiconductor pixel-array detectors have found many applications in the field of scientific and medical imaging. For radiation imaging applications, the hybrid pixel detector is increasingly gaining importance. In such devices, a pixel detector material is bonded to read-out electronics circuits. Various detection methods have been used, whereas the readout is usually implemented in CMOS technology as integrating or single photon processing pixel detectors. Single Photon processing pixel circuit includes analog and digital processing channels. The analog channel consists of a preamplifier, a pulse shaping amplifier and comparators in addition to pulse pile-up rejecters and base-line restorers. The digital part consists of pulse discrimination logic, counters and associated read-out logic. Unlike the integrating type, which contains a small number of transistors, single photon processing pixels contain complex circuitry. This makes the pixel circuit design mainly driven by area, power consumption, and mixed mode design constraints. The restriction of the area comes from the system requirement on the spatial resolution of the pixel array detector. The continuously ongoing downscaling of the CMOS technology makes it possible to include more advanced processing circuits in the pixels. Recent developments in digital technology, it is possible to include more advanced processing circuitry embedded in the pixels. In a state of the art single photon processing pixel array [1] each pixel cell is 55 um x 55 um and contains approximately 500 transistors in 0.25 mm CMOS technology. Charge sharing in imaging detectors is a problem that becomes increasingly severs as the pixel dimension shrinks. For small pixel sizes the lateral broadening of the charge will be significant and charge from a single hit may be detected in a neighborhood of pixels. This effect may limit down scaling of pixel sizes in single photon processing detectors as it limits the spatial resolution and distorts the energy spectrum.

This paper proposes a mechanism for suppressing the charge sharing. For this, additional circuits are introduced. The additional circuit is containing the digital part shared between each four pixels; this will allow the pixel to have only analog part. The mechanism leads to reduce the area (number of transistors) and also leads to reduce the effect of digital swished noise, as presented in [7]. A generalized functional description is presented that supports arbitrary pixel configuration.

2. Photon Counting Pixel Arrays

A typical single photon processing readout pixel electronics presented in [2] consists of analog front-end electronics and digital electronics for counting events (see Figure 1). The pre-amplifier is a Charge Sensitive Amplifier [3]. The Shaper [4] enables the system bandwidth to be

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reduced and thus reduces the noise in the detected signal before discrimination. The signal is fed to two analog comparators that output binary signals (LT and UT) indicating whether or not the signal exceeds the threshold values. A conditionally generated clock signal to the event-counter (EC) is generated by the All-Digital Window Discriminator (ADWD) on the basis of the sequences of UT and LT. The ADWD is a simple asynchronous controller generating the clock signal without reference to either internal or external timings. The event-counter is a Linear Feedback Shift Register (LFSR) consisting of 14 bits. It is built on dynamic Flip-Flops with a single-phase clock and each consisting of six transistors.

The pixel consists of a total of 215 transistors of which 112 are for the digital part. The idle power dissipation (static) is 1.6 mW and the analog part is its main contributor. The active power, when an event is detected, is 3.6 mW. The pixel has been implemented in a 120 nm CMOS technology which operates at 1.2 V.

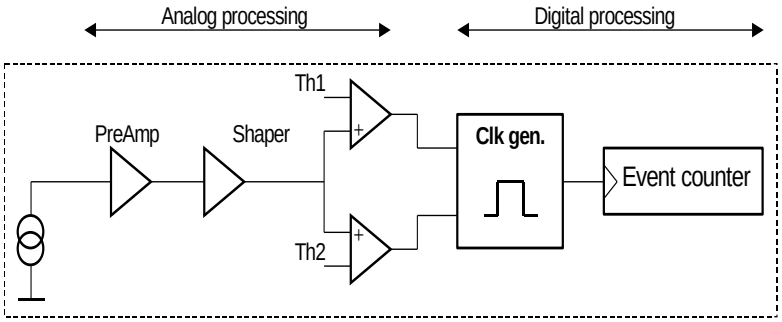

Figure 1. Pixel for photon counting image sensors

3. Charge Sharing

When using the single photon processing method with very small pixel cells (less than about 100 um size), the phenomenon of charge sharing [5] has to be addressed. However, there are concerns that as the size of pixel is reduced, the sharing of charge between neighboring pixels becomes more pronounced. The basic idea of the proposed charge-sharing mechanism is to localize detected charge, which may be distributed over several pixels to one single pixel where all charges from the neighboring pixels are summed. Figure 2 illustrates the different cases in a four pixel summation configuration.

The gray shaded regions represent “charge-clouds” and the pixels marked with ‘X’ are those in the center of the charge where all charges detected in their respective neighborhood are added. Let us consider a special case to illustrate the principles of the proposed charge-sharing suppression technique. In Figure 3 a neighborhood of four pixels is considered. A pixel is communicating with its neighbors by sending its detected charge represented by either voltages or currents to Sum function ($sum_{i,j}$) and Evaluation Function ($EF_{i,j}$).

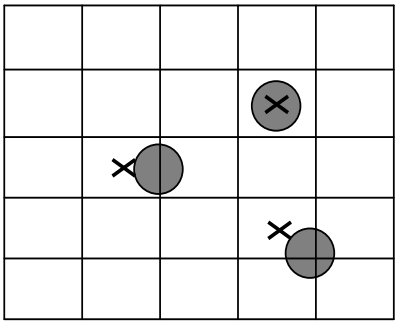

Figure 2. Illustration of charge-sharing mechanism

Consequently the Function will receive detected charges from Four pixels ($c_{0,0}$, $c_{-1,0}$, $c_{-1,1}$, $c_{0,1}$, $D_{0,0}$, $D_{-1,0}$, $D_{-1,1}$, $D_{0,1}$)

Given this information from the neighbors, Sum and EF can perform the following:

1. Sum the detected charges in a neighborhood
2. Determine if the detected charge in the pixel is greater than the ones detected in the other pixels in the neighborhood.

By implementing these two functions, we are able to localize all detected charge distributed in a neighborhood, to one single pixel. This pixel is the one that detected the greatest charge in its neighborhood.

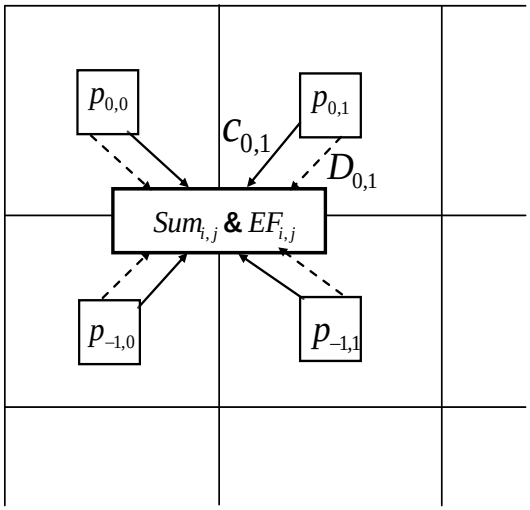

Figure 3, Example of four pixels communication scheme

The size and shape of the neighborhood may be designed according to design criteria such as circuit complexity, power consumption and assumption on the spatial extension of the charge clouds to be detected.

In general, we consider a pixel array P of n x m pixel elements defined as:

$$P = \begin{bmatrix} P_{0,0} \cdots\cdots P_{0,m-1} \\ \vdots \\ .P_{n-1,0} \cdots\cdots P_{n-1,m-1} \end{bmatrix} \quad (1)$$

where $P_{i,j}$ is the pixel element, $i \in \{0,.....,m-1\}$, $j \in \{0,.....,n-1\}$ in the set P.

A neighborhood of pixels of pixel $p_{i,j}$ is defined as:

$$N_{i,j} \subseteq p \quad (2)$$

where $P_{i,j} \in N_{i,j}$ For inter pixel communication, the detected charge in pixel $P_{x,y} \in N_{i,j}$, denoted $C_{x,y}$ is used.

A pixel $P_{x,y}$ sends its $C_{x,y}$ to the summation function $sum_{i,j}$ in pixel $P_{i,j}$ .this summation is defined as:

$$sum_{i,j} = \sum_{N_{i,j}} C_{x,y} \tag{3}$$

The detected charge in the pixels $P_{x,y} \in N_{i,j}$, send it $D_{i,j}$ to the $EF_{i,j}$, then $EF_{i,j}$ receive four clock signals from four comparators which use common threshold, the function of the common threshold comparators is defined as:

$$D_{i,j} = \begin{cases} 1 & if \quad (C_{ij} > th_{com}) \\ 0 & otherwise \end{cases} \tag{4}$$

The evaluation function is used to evaluate if a particular pixel in the neighborhood is the one with the largest charge. However, the decision has to be set. The outputs of $D_{i,j}$ are the clock signals generated depending on the value of the neighborhood charge signals with respect to the common threshold. They are fed to the evaluation function. The Evaluation Function $EF_{i,j}$ located between the pixels is defined as:

$$EF_{i,j} = \begin{cases} out\_di = 0 & if\ clk\ \ 1 \\ = 1 & if\ clk\ \ 0 \end{cases} \tag{5}$$

By incorporating $EF_{i,j}$ and $sum_{i,j}$ function between each four pixels in the single photon processing pixels array, a charge-sharing suppression mechanism can be realized. The pixel proposed in this paper is depicted in Figure 4.

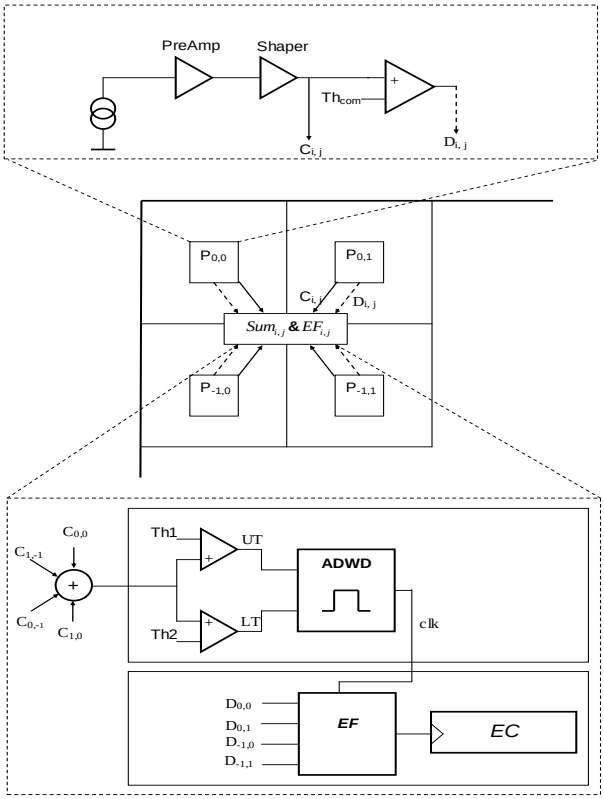

Figure 4 proposed architecture

The sum of all detected charges $sum_{i,j}$ in the neighborhood is fed to two comparators The function of the thresholds for the comparators is to be able to generate a clock signal depending on the value of the signal and the threshold value is:

$$LT = \begin{cases} 1 & if \quad (sum_{i,j} > th1) \\ 0 & otherwhise \end{cases} \tag{6}$$

$$UT = \begin{cases} 1 & if \quad (sum_{i,j} < th2) \\ 0 & otherwhise \end{cases} \tag{7}$$

By setting the global threshold values such that th2 > th1, energy window discriminator of the $sum_{i,j}$ can be made. The window discrimination is made on this $sum_{i,j}$ by first comparing the magnitude with Th1 and Th2 values. As a result, sequences of binary events will appear on the outputs of the comparators UT and LT are used for performing window discrimination in All-Digital Window Discriminators (ADWD). Three different sequences of events on UT and LT are possible:

$sum_{i,j} < th_1$: No event on UT and LT; (8)

$$sum_{i,j} > th_2 : LT^+ \rightarrow UT^+ \rightarrow UT^- \rightarrow LT^- \tag{9}$$

$$th_1 < sum_{i,j} < th_2 : LT^+ \rightarrow LT^- \tag{10}$$

The event to be detected is described in case 10.

Based on these sequences of events a self-timed circuit can be designed to generate a clock signal (clk) only when the signal remains within the defined window. Further details on the design of the ADWD are presented in [6].

Evaluation Function $EF_{i,j}$ creates a counter for each $D_{i,j}$ input which is used as clocks. When all the $D_{i,j}$ input signals are low at the positive edge of the clk clock input, the values of the counters are compared to find the pixel with the largest charge in the neighborhood. The pixel with the largest charge is given the maximum value (65535 in 16-bit pixel resolution) whereas the other pixels are given the minimum value (zero). All counter values will then be reset to zero and new counting can begin. Counters and outputs are reset to zero whenever the reset signal is high.

4. Results

To analyze charge-sharing events in photon counting pixel detectors, the input charges were performed in Candace Analogue Simulator and the results were used as inputs to a hardware module. The module was designed to be sensitive to four neighboring pixels charges. For simulation purposes, Test-bench and Top module were implanted to create a complete simulation environment.

The charge sharing control system can be build using the information coming from the four neighboring pixels and the information obtained by comparing the ratio of the pixels charges. In Figure 5, the four signals are about (35%, 25%, 20%, and 15%) of the input charge and summing output.

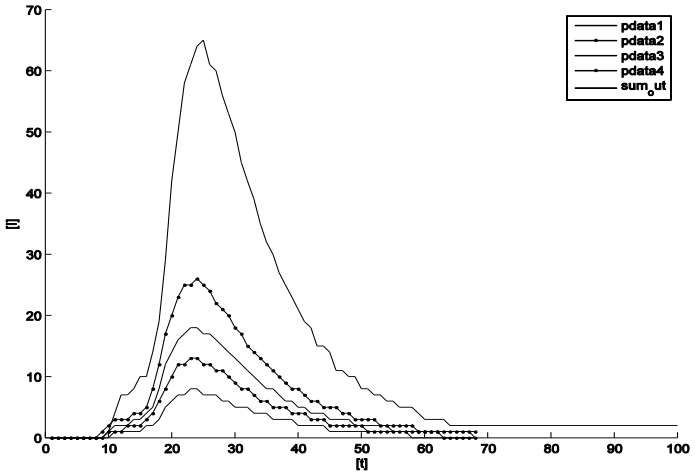

Figure 5, simulated input charges are about (35%, 25%, 20%, and 15%) of the input charge and the summing output.

In Figure 6, the upper plot represents the summing output. The lowers signals are a binary signals that generated by the comparators and ADWD. The pulse is within the two threshold values UT and LT, which defines the energy window of interest

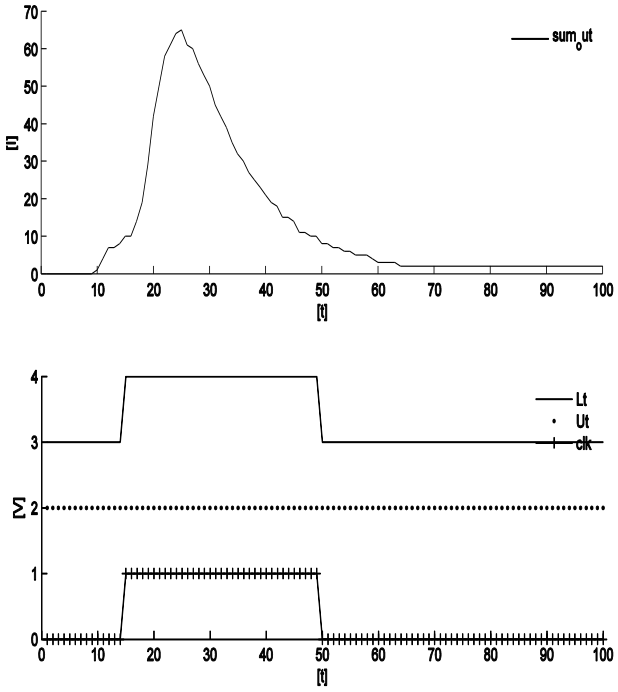

Figure 6 Sum out, window Discriminator and ADWD outputs

Figure 7 shows the output charges of the 4 neighboring pixels and the 4 common thresholds comparators outputs. The upper plots represent the charges of the 4 neighboring pixels. The lowers signals are a binary signals that generated by the common thresholds comparators, and the clock signal for counting the pulses.

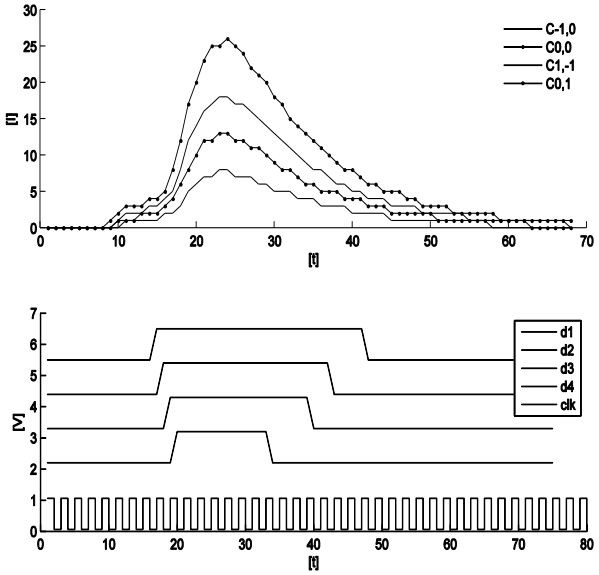

Figure 7, output charges of the 4 neighboring pixels and the 4 common thresholds comparators outputs, and clock

5. Conclusions

In this paper we have introduced a mechanism for suppressing charge sharing. This mechanism has been incorporated in a photon counting pixel detector. The functionality of the pixels and their interaction are modeled in VHDL. By having the decision of center-of charge residing locally within each of the pixels, it is reliable and its performance is only limited by process variations within the neighborhood of pixels. The proposed architecture, given in Figure 4, facilitates straightforward circuit implementation

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