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Design of Power-Efficient Structures of the CAM Cell using a New Approach in QCA Nanoelectronics Technology

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is a new emerging nano-electronic technology. Owing to its many favorable features, such as low energy requirements, high speed, and small size, QCA is being actively suggested as a future CMOS replacement by researchers. Many digital circuits have been introduced in QCA technology, most of them aiming to reach the function with optimum construction in terms of area, cell count and power consumption. The memory circuit is the main building block in the digital system therefore the researchers paid attention to design the memory cells with minimum requirements. In this paper, a new methodology is introduced to design two forms of CAM cells. The proposed designs required two 2:1 multiplexers, one OR gate and one inverter. The first proposed design reduces the power consumption by 53.3%, 35% and 25.9% at (0.5 Ek, 1 Ek, and 1.5 Ek) while the second design by 53.2%, 31.9% and 20.5% (0.5 Ek, 1 Ek, and 1.5 Ek) respectively.

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1. INTRODUCTION

Power consumption is an important issue in digital system design. Any new technique that comes to consideration has to be competitive in terms of power consumption. Quantum-dot Cellular Automata (QCA) is a modern nano-technique that is emerging as a new prominent alternative to CMOS technology, promising low energy consumption levels. QCA was first introduced by Lent et al [1]. In QCA, the binary values are represented by electrons position rather than by voltage levels like in CMOS [2]. The primary building block in QCA is a square cell that contains four quantum dots injected with two electrons. The electrons can tunnel between dots according to the principle of electrons repulsion. Circuit complexity is another important issue in digital system design, especially in QCA, and although many important forms of memory circuits were proposed in QCA technology such as [3-9], a lot of optimization is still needed. Content addressable memory (CAM) is a high-speed type of memory that is utilized in many applications such as network routers and switches. A CAM cell is at the core of the implementation of such memory architecture, hence, it is in the focus of many researchers interested in QCA technology [3-5]. In this paper, a new approach for CAM cell design is proposed. The new design is based on two multiplexers, this make it very efficient on the gate levels and very abstracted compared to the available designs. The proposed approach is used to construct two novel structures of a QCA-CAM cell. These structures are carried out with a significant reduction in power consumption. QCADesigner tool v 2.0.3 [10] is used for the design and verification of the circuit, while QCAPro [11] is used as the power analysis tool.

2. BACKGROUND

2.1 QCA fundamentals

The primary QCA cell consists of four dots injected by two electrons. Due to the principle of electron repulsion, the electrons settle in diagonal positions. A QCA cell has only two configurations depending on the driver cell as illustrated in Figure 1. A cell with polarization equal to "-1" represents binary "0", while a cell with polarization "+1" represents binary "1" [12]. The polarization of a cell can be calculated using Equation 1.

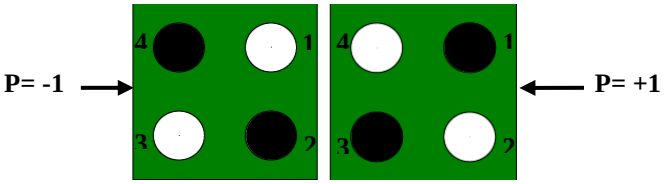


Figure 1. QCA cell configurations

$$p = \frac{(p1+p3)-(p2+p4)}{p1+p2+p3+p4} \quad \text{. . . Equation 1}$$

Where pi represents the availability of an electron inside a dot. A binary value is transferred from the input to the output using a QCA-wire. A QCA-wire consists of a set of QCA cells arranged in a line connecting two points. The Coulomb interaction forces the electrons in an adjacent cell to modify their positions depending on driver cell. The modified cell, then, becomes a driver cell for the next one inline and so on. Eventually, the last cell in the arrangement, the output cell, will have the same polarization as the input cell. The QCA binary wire is illustrated in Figure 2. A crossover could be performed by rotating one wire at 450 or by using the approach proposed in [13].

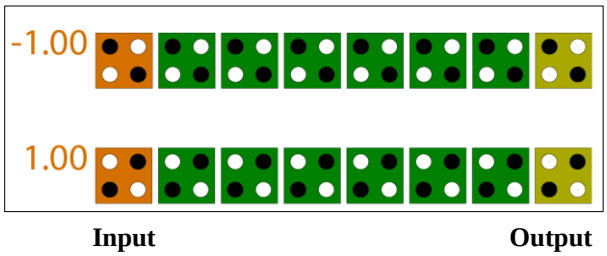


Figure 2. QCA binary wire

The building blocks of QCA circuits are the majority gate and inverter. Figure 3 shows a 3-input majority gate (Maj-3). A majority gate gives a "1" at the output when most inputs are ones, and it gives a "0" when most inputs are zeroes. AND and OR logic gates can be designed in QCA using a 3-input majority gate by fixing one of the inputs. If fixed input is at logic "1", the majority gate would operate as an OR gate. Alternately, if the fixed input is at logic "0", the majority gate would represent an AND gate. The majority gates of multiple inputs have attracted the attention of many researchers [14-17] while its reliability is discussed in [18]. Inverter block is also an important component in designing circuits in QCA. A couple of inverter configurations are shown in Figure 4. Although the inverter of Figure (b) is theoretically operational, it could be affected by adjacent cells crosstalk and there is a high probability of failure, hence, the inverter in Figure (a) is preferred due to its robustness [19].

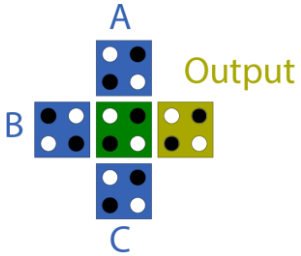


Figure 3. QCA 3-input majority gate

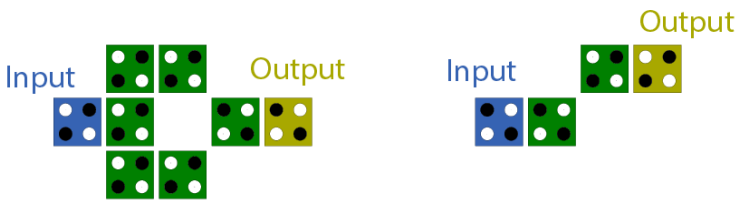


Figure 4. QCA Inverter configurations

Synchronization in QCA circuits is done by the use of clock signals. The clock signal is instrumental for circuit stimulation and data flow control. The clock signal controls the barriers between the dots to allow or prevent the electrons tunneling between dots inside a cell. QCA circuit operation is controlled typically using four clock signals dividing the circuit into many zones, each zone contains four phases (relax, switch, hold, and release), as shown in Figure 5, so as to maintain the circuit close to ground state and provide adiabatic switching [20].

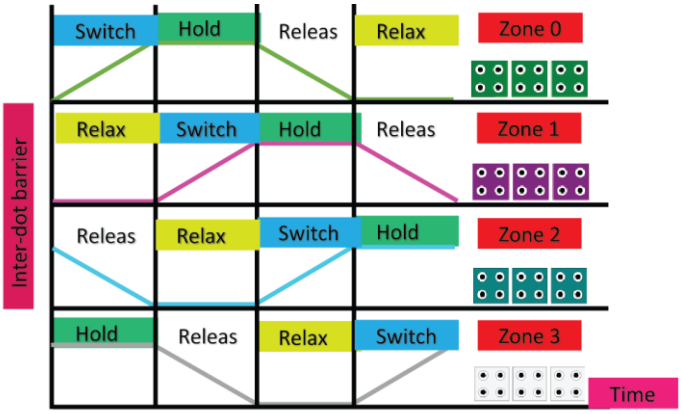


Figure 5. Clock signal phased in 4 zones

2.2 CAM Memory

Content addressable memory (CAM), alternately called associative storage, utilizes a different searching strategy to that of Random-Access Memory (RAM). In CAM, the data is collected by giving its content rather than address. Instead of getting data from one address like in RAM, the CAM architecture searches the whole memory for matching data in one cycle; therefore, it yields a very fast operation, consequently, making it suitable for applications that prefer the speed to justify the overhead in cost and complexity. A block diagram representing a CAM cell is shown in Figure 6.

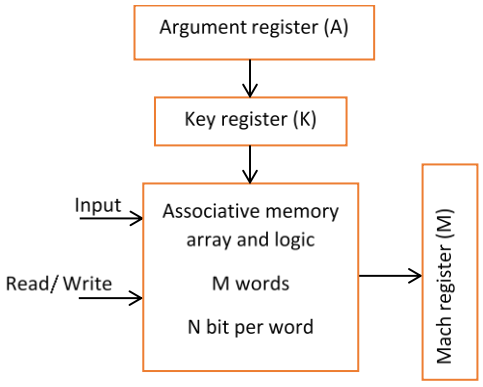


Figure 6. Block diagram of organization of CAMs

QCA based CAM cells were presented previously using two different approaches. The first approach is based on a 5-input majority gate implementation such as that of Figure 7 [3]. The second approach is based on XOR gate implementation as shown in Figure 8. As explained in the contoured areas (red frames) in figures 7 and 8. Lower complexity is a desirable property, but it should not be with the cost of lower robustness. These

CAM cell designs have a high fault rate in practical scenarios. In CAM, the data entered is compared to the stored memory arrays looking for matching data to return its address. The CAM circuit consists of two main parts, memory part and matching part [4]. The memory part receives data input and (READ/WRITE) signal. The matching part gets the memory cell content (indicated as F) accompanied by the argument (indicated as A) as well as key signals (indicated as K). This construction sets the match signal (indicated as M) if the queried data existed [4].

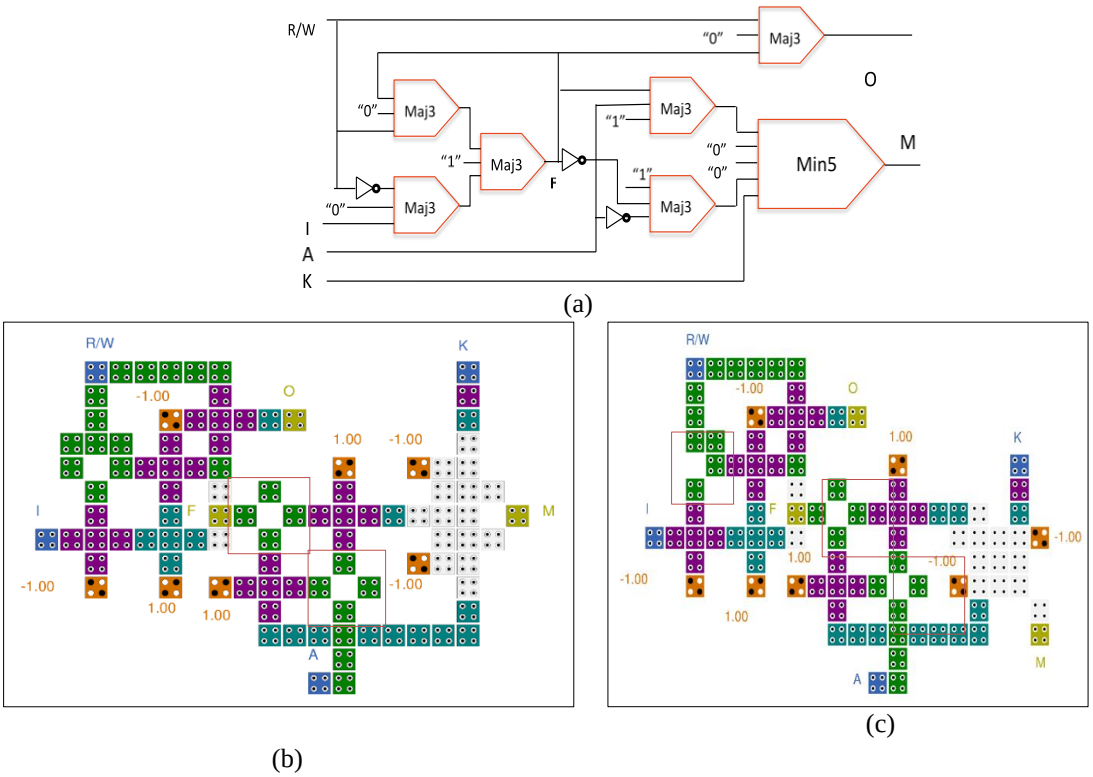


Figure 7. CAM cells introduced previously based on Maj-5 (a) Block diagram in [3] (b) QCA layout in [3](c) QCA layout in [4]

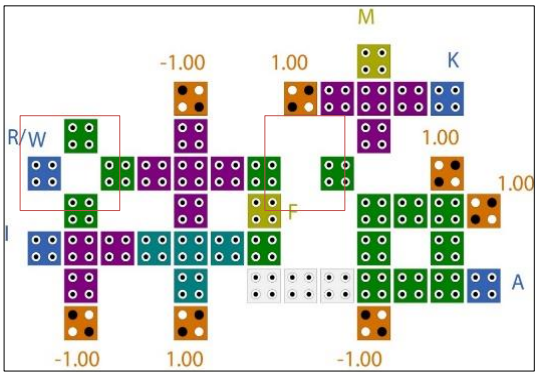


Figure 8. QCA-CAM cell introduced in [5]

3. PROPOSED DESIGN

In this section, a new approach for designing a CAM cell is proposed. The proposed circuit is accomplished using two 2:1 multiplexers, one inverter, and one OR gate. Figure 9 illustrates the block diagram of the proposed CAM cell.

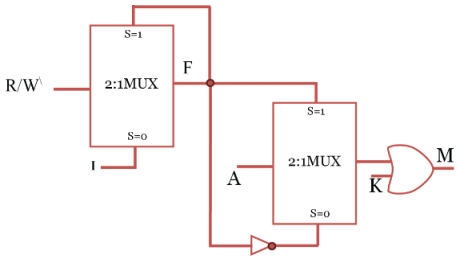


Figure 9. The proposed diagram of the CAM cell

The strength of the proposed approach can be demonstrated by QCA technology, in which two novel structures of QCA-CAM cells have been constructed. The first structure is superior in all metrics while the second one is more robust than previously reported designs in the literature.

The QCA layouts of the proposed CAM cells is illustrated in Figure 10. The 2:1 multiplexer utilized in this paper is proposed in [21]. The first proposed circuit utilizes 39 QCA cells only, while the second proposed circuit utilizes 43 cells but it uses the robust inverter form. **Equation 2** is the formula used for the memory part operation, while **Equation 3** is used for the matching part operation.

$$F^*=I(R/W)^{\}+F(R/W)} \quad \text{. . . Equation 2}$$

$$M=K+\overline{K}\left(AF+\overline{A}\overline{F}\right) \quad \text{. . . Equation 3}$$

where F* represents the next state of F (memory content), I is input, M is match data, K is a key signal and A is an argument signal. In the memory part, to perform a write operation, the R/W signal is to be set to 0, then, the input data would be moved to the output (F). If 1 is set on the R/W signal, no change to (F) would occur as detailed in Table 1. In the proposed approach, this operation is carried out by the first multiplexer where (R/W) represents the selector of the multiplexer.

In the matching part, the argument (A) represents the selector of the second multiplexer to control the match output (M) as detailed in Table 2. The key signal (K) is acting as a global control (enable) for the entire input/output association process.

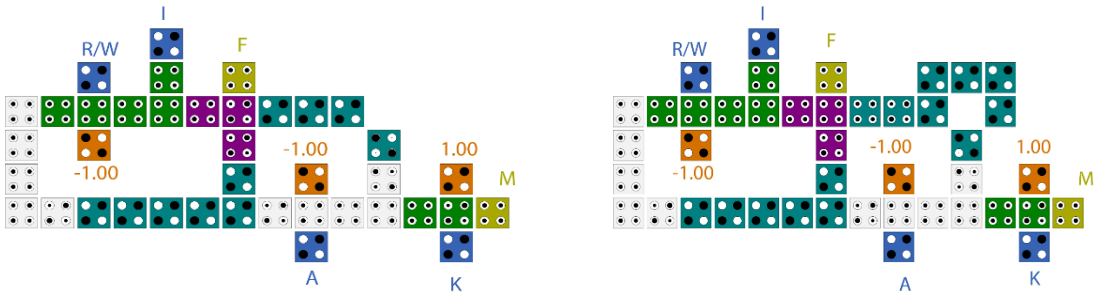
Table 1. Memory operation

Input (I)	R/W signal	F(t)	F(t+1)	Operation
1	0	x	1	Write
0	0	x	0	Write
X	1	0	0	Read
X	1	1	1	Read

Table 2. Mach operation

K	A	F (t)	M
1	x	x	1
0	0	1	0
0	0	0	1
0	1	1	1
0	1	0	0

Based on the proposed approach, two CAM cell structures are proposed with QCA technology, one with reduced inverter and the other with a robust inverter. Changing the inverter type did not add noticeable overhead in terms of power consumption, latency and circuit size.



(a) (b)

Fig. 1. The proposed layout of QCA-CAM cell using (a) corner inverter (b) robust inverter

4. SIMULATION RESULT

The proposed CAM cell design was simulated using QCADesigner tool v2.0.3. This tool was set with the default simulation parameters. The waveforms of the input-output for the proposed CAM cell are shown in Figure 11. The resulted waveforms show that the proposed design is fully operational and free of errors and the circuit operates as expected. Table 3 compares the proposed design against the other published solutions in terms of QCA cell count, cell area, and latency. The first proposed design is superior in almost all metrics while the second proposed design is the more robust layout.

Table 3. CAM cell comparison

CAM cell	Number of cells	Area (μm^2	Latency (clock cycles)
Maj-5 based CAM cell [3]	100	0.14	2
Maj-5 based CAM cell [4]	94	0.11	2
XOR based CAM cell [5]	46	0.04	1.5
1st Proposed CAM cell	39	0.04	1.25
2nd proposed CAM cell	43	0.04	1.25

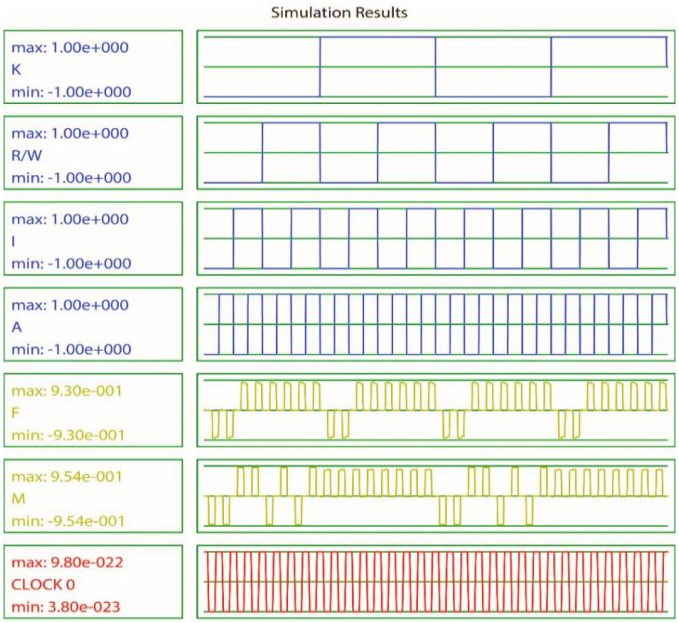


Figure 2. Output waveforms of the proposed CAM cell

5. POWER CONSUMPTION ANALYSIS

Power consumption is a very important metric in digital system design, especially in nano-electronics technology. Many papers in the literature presented the same circuit in QCA technology but the focus was on reducing power consumption [22-28]. In this work, the analysis of power consumption is performed to prove the trustworthiness of the proposed design. The signal is moved using the principle of the Coulomb interaction. So, the total energy between two adjacent cells (m, n) can be calculated using Equation 4,

$$E_{i,j} = \frac{1}{4\pi\epsilon_0\epsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_{i,n}q_{j,m}}{|r_{i,n}-r_{j,m}|} \quad \text{… Equation 4}$$

where q is the signed magnitude of the electric charge, $|r_{i,n} - r_{j,m}|$ represent the distance between electron i in cell m and electron j in cell n, ϵ_0 is the permittivity of vacuum and ϵ_r is the relative dielectric permittivity [29].

For better analysis and comparisons, the QCAPro tool [11] will be used. This tool has the capability of expecting the losses of power for a large number of cells in non-adiabatic switching because it uses the fast approximation-based technique method. A comparative analysis of dissipated power for the proposed QCA based CAM cell is shown in Figure 12. This comparison is done in different energy levels (0.5Ek, 1Ek, and

1.5Ek) with temperature value 2k. The dissipated power maps for the proposed structures at 0.5Ek tunneling energy are depicted in Figure 13.

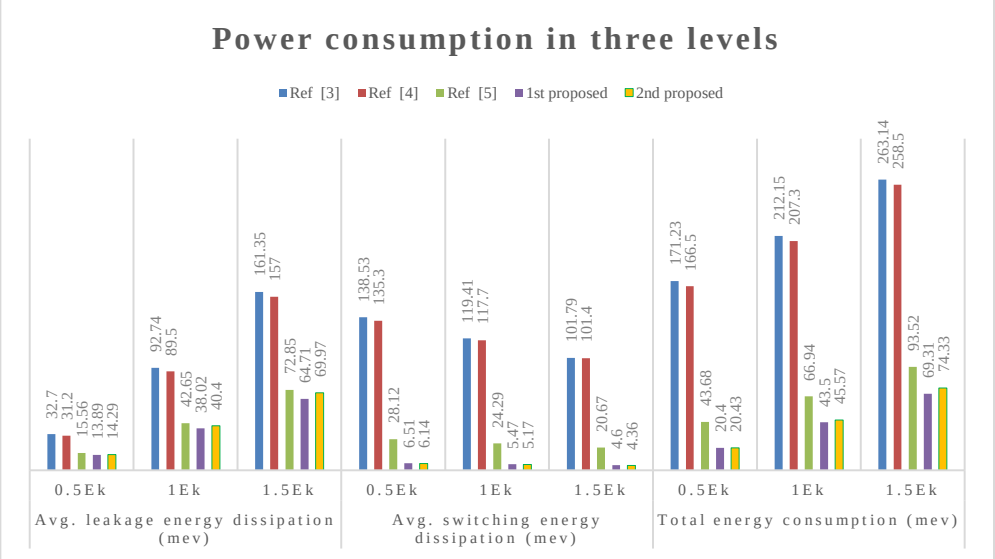
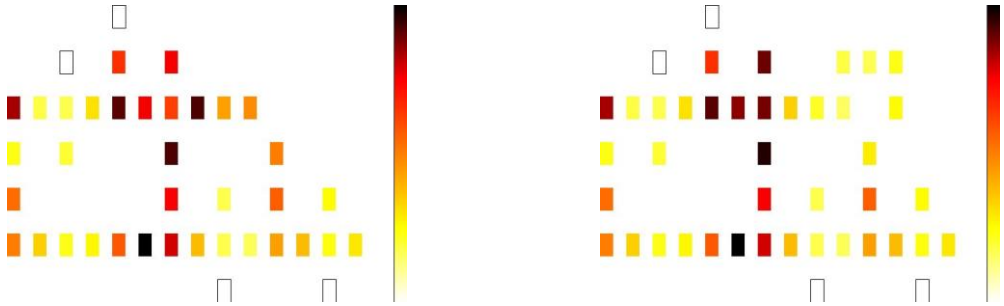


Fig. 3. Power consumption comparison of CAM cells



(a) (b)

Fig. 4. Thermal map for proposed CAM cells at 0.5 Ek using (a) corner inverter (b) robust inverter

The circuits were analyzed at three stages (0.5 Ek, 1 Ek, and 1.5 Ek). Power analysis indicates the superior efficiency of the proposed CAM cell design. The first proposed design made a collective 53.3% relative improvement over [5] in terms of total energy consumption at 0.5 Ek, and made a 35% advantage at 1 Ek while achieving a 25.9% improvement at 1.5 Ek. The second proposed design made a collective 53.2% relative improvement over [5] in terms of total energy consumption at 0.5 Ek, and made a 31.9% advantage at 1 Ek while achieving a 20.5% improvement at 1.5 Ek.

6. CONCLUSION

QCA technology is a promising technology presented to be a good replacement for CMOS technology. Memory circuits are so important in digital systems therefore many papers focus on designing new structures hoping that it will be optimal. In this paper, a new methodology for CAM cell design has been proposed. Using the proposed methodology, two different structures of QCA-CAM cells was presented. The first proposed design, discussed here, proved to be superior to other related work circuits in almost all comparison metrics. The second proposed CAM cell utilizes the robust inverter to reduce the fault rate although it takes a slight increase in cell count.

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