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Investigation of TTMC-SVPWM Strategies for Diode Clamped and Cascaded H-bridge Multi-level Inverter Fed Induction Motor Drive

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Abstract

This paper presents a concept of two types multilevel inverters such as diode clamped and cascaded H-bridge for harmonic reduction on high power applications. Normally, multilevel inverters can be used to reduce the harmonic problems in electrical distribution systems. This paer focused on the performance and analysis of a three phase seven level inverter including diode clamped and cascaded H-bridge based on new tripizodal triangular space vector PWM technique approaches. TTMC based modified Space vector Pulse width modulation technique so called tripizodal triangular Space vector Pulse width modulation (TTMC-SVPWM) technique. In this paper the reference sine wave generated as in case of conventional off set injected SVPWM technique. It is observed that the TTMC-Space vector pulse width modulation ensures excellent, close to optimized pulse distribution results and THD is compared to seven level, diode clamped and cascaded multi level inverters. Theoretical investigations were confirmed by the digital simulations using MATLAB/SIMULINK software.

Keywords*: Seven level Diode clamped and cascaded inverter, SPWM, TTMC-SPWM, TTMC-SVPWM, TTMC-SVAPODPWM, THD.*

1. Introduction

In the region of high voltage and power, a high quality inverter fed ac drive is more easily obtained by the use of multi-level and in the first turn of three-level - inverters. And the several PWM methods for this inverter have been elaborated previously [1-2]. The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. The unipolar PWM and space vector PWM are the most preferred pwm control techniques. Even though space vector modulation (SVM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation. Different aspects of the three-level inverter will be discussed including the inverter topology [3-4].

Another important topology, named Cascade H-Bridge (CHB), has fewer components to achieve the same number of output voltage levels. It is one of the most widely used topologies due to its reliability and increased capacity to operate under fault conditions in the cells [5-6]. Regarding the modulation techniques, these can be divided into two groups: time domain modulation, better known as pulse width modulation (PWM), and space vector modulation (SVM). Within the group of time domain, the phase-shift modulation (PSPWM) is the most known, having a triangular carrier and a sinusoidal modulator for each phase, which both are compared and determine how each leg to operate and is widely used in inverters for its simplicity [7-8].

This paer focused on the performance and analysis of a three phase seven level inverter including diode clamped and cascaded H-bridge based on new tripizodal triangular space vector PWM technique approaches. In this paper the reference sine wave generated as in case of conventional off set injected SVPWM technique. And comparision of THD for both multilevel inverters.

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2. Three-Phase Seven-level Diode Clamped and Cascaded Multi-level Inverter

The structure of a multilevel converter based on series of inverters three phase H-bridge ; sinusoidal wave voltage is produced by a series of connected H-bridge inverters. Each cell of the inverter is supplied by a source DC. The structure of a seven-level inverter arm cascaded type H-bridge is associated with cascade three leg three-phase inverter. Each H-bridge contains four active switches P_1 to P_4 with anti-parallel diodes D_1 to D_4. The separate DC volt- ages sources are set to 100 V for each H-bridge and the switching frequencies are 1KHz for triangular carrier waves. This type of multilevel inverter topologies can reduce the number of switching devices, but it requires multiple isolated dc supply to operate the converter.

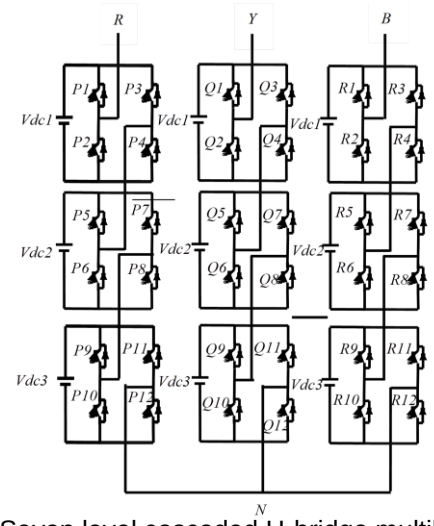


Figure 1. Seven level cascaded H-bridge multilevel inverter

Figure 1 Exposes out to us the three-phase seven level cascaded H-bridge inverter. In cascaded H-bridge, each low voltage h-bridge portion has its own DC-link voltage source. Its control structure is performing much better than NPC inverter. This inverter is common with other inverters in having seven level. This inverter includes 3 H-bridges inverters that are connected in one lag cascaded form. The 7-level cascaded H-bridge has been built using 12 switching devices[9].The three phase seven level neutral point clamped inverter (NPC) or Diode clamped Multi level inverter (DCMLI) topology shown in Figure 2.

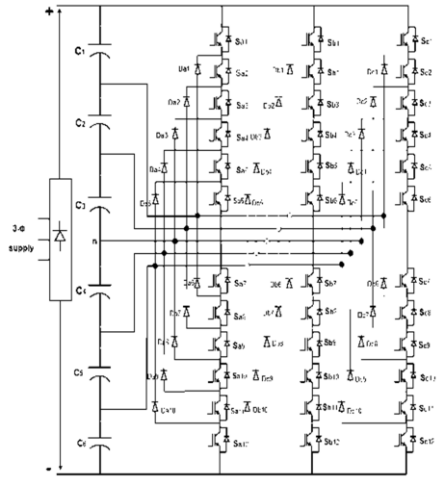


Figure 2. Seven level diode clamped (NPC) multilevel inverter

The main feature of the NPC topology is that it requires only one DC source similar to two-level in high power applications, the structure is most suitable, compared to the conventional structure. The voltages and current outputs have a much lower harmonic distortion inverter. Moreover, it provides better performance [10]. In Figure.2, we show three-phases of seven-level diode clamped inverter.The seven-level can be achieved by using 12 switches ; each phase is consisted of (6 switches for high leg and 6 switches for bottom leg). The three-phase shares common dc bus. The clamping diode can be used to restrict safe working level for the voltage across each capacitor. Therefore, the m-level diode clamped inverter has a (2m-1)-level output voltage and an m-level output phase voltages [11].

3. Generalized TTMC- Space Vector PWM Technique for Cascaded H-bridge and Diode Clamped Multilevel Inverter

The sub-harmonic pulse width modulation (SPWM) is commonly used in industrial applications. The frequency of reference singnals fr determines the inverter output frequency fo ; and its peak ampltiude Ar controls the modulation index M. Figure 3. Demonstrates the sine-triangular method for three-phase seven level inverter. There in the a phase modulation singnal is compared with six (n-1in general) triangular waveforms [12]. For a seven level inverter it requires 6 triangular carriers.

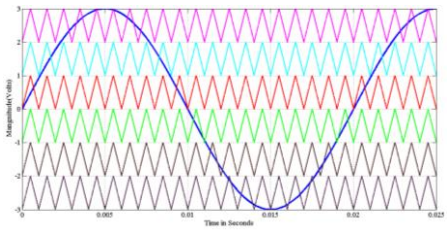


Figure 3. PD-SPWM

A novel trapezoidal triangular carrier has developed by adding triangular off set to sinusoidal fundamental waveform so as to shift the lower order harmonics to higher order side. This novel carrier is compared with the offset injected space vector reference waveform to generate the required PWM pulses to the inverter. To analyze the performance of the proposed PWM technique it is implemented on seven level cascaded and diode clamped Multi-level Inverter. In conventional SVPWM for multilevel inverters to find the switching time duration, for different inverter vectors, the mapping of the outer sectors to an inner sub hexagon sector is to be done. The switching inverter vectors corresponding to the concrete sectors are switched and the time periods premeditated from the mapped inner sectors. Implementing such a scheme in multilevel inverters will be very difficult, because higher number of sectors and inverter vectors are present. And in this method the computation time is increased for real time application. In carrier based PWM scheme aproper offset voltage is added to sinusoidal references before comparing with carrier waves, to attain the performance of a SVPWM [13].

$$Toffset = \frac{-(T\max + T\min)}{2} \quad (1)$$

T_a,T_b and T_c are the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages.Then, the comparison between the phase voltages maximum and minimum absolute values allows the identification of which reference is responsible for switching in each half period of the carrier. For this purpose, the modulus function is used to move vertically the reference voltages, resulting in a common point between the carriers intersections[14]. This function is given in equation (2), (3), (4).

$$Ta = \frac{-(Va * Ts)}{Vdc} \quad (2)$$

$$Tb = \frac{-(Vb * Ts)}{Vdc} \quad (3)$$

$$Tc = \frac{-(Vc * Ts)}{Vdc} \quad (4)$$

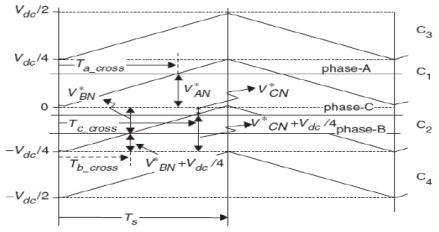
An important detail is taken into account to avoid the function operating in negative values, which makes use of another offset in the reference voltage [15]. Thus, substituting equation (2), (3), (4) into equation (1) and adding this offset, the equation (5), (6), (7) is obtained.

$$Toffest = [\frac{To}{2} - T\min] \quad (5)$$

$$To = [Ts - Toffest] \quad (6)$$

$$Toffeset = [T\max - T\min] \quad (7)$$

Figure 5, Figure 6, and Figure 7 is shown in the waveform results generated by adding the offset voltage described in with the reference sinusoidal waveform. Figure 4. is shows the comparision of SPWM technique and minimum maximum techniques.



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igure. 4.Comparision of SPWM technique and minimum maximum techniques

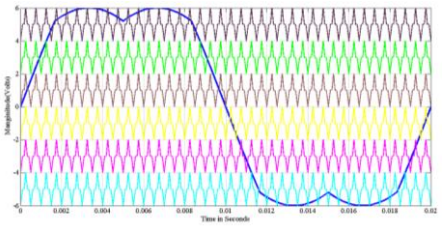

Figure 5. TTMC-PDSVPWM

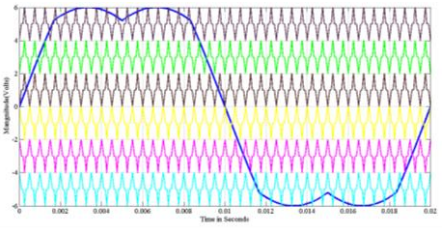

Figure 6. TTMC-PODSVPWM

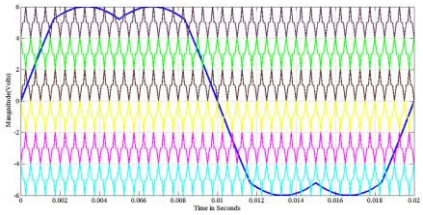

Figure 7. TTMC-APODSVPWM

4. Simulation Results and Discussion

The simulation study has performed and carried out three-phase multilevel inverters behavior based on comparative regrding two different of three-phase diode clamped and cascaded H-bridge multilevel inverters were developed and its parameters as shown in table1. In this simulation the constant tripizodal triangular carrier based space vector PWM technique was used. The carrier frequency used in this designed is about 1 KHz.

4.1. Cascaded H-bridge Multilevel Inverter Simulation Results

The seven level CHBMLI we have done matlab simulation using SPWM techniques (PD-SPWM, POD-SPWM and APOD-SPWM). We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter show in Figure 8., Figure 9. And Figure 10. In the seven level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the PD-SPWM techniques is perfect with the low THD, voltage and current shapes of the seven level CMLI.

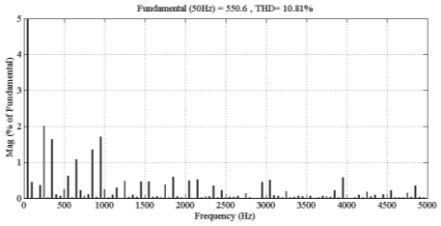

Figure 8. THD for CHB_PDSPWM

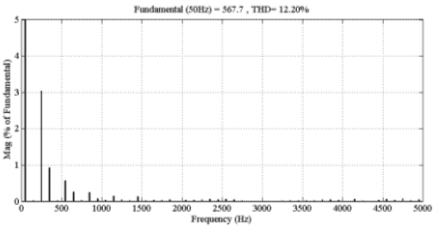

Figure 9. THD for CHB_PODSPWM

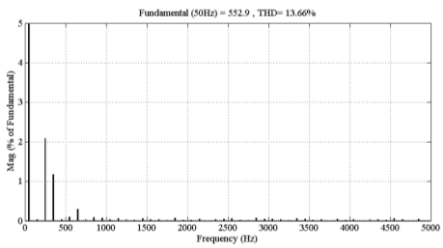

Figure 10. THD for CHB_APODSPWM

The seven level CHBMLI we have done matlab simulation using Tripizodal tringular carrier based SPWM techniques (TTMC-PDSPWM, TTMC-PODSPWM and TTMC-APODSPWM). We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter show in Figure 11., Figure 12. And Figure 13. In the seven level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the TTMC-PDSPWM techniques is perfect with the low THD, voltage and current shapes of the seven level CMLI. And we can observe the performance of THD is low in case TTMC based SPWM comparision of trianular carrier based SPWM techniques.

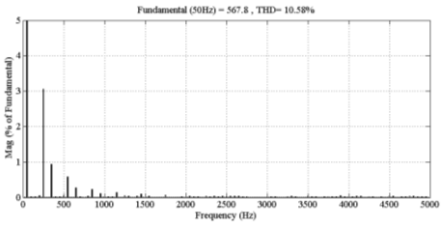

Figure 11. THD for CHB_TTMC_PDSPWM

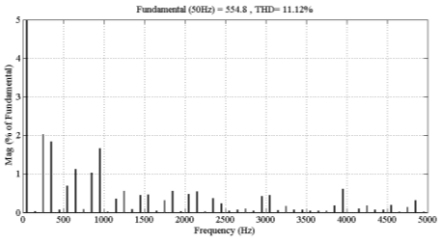

Figure 12. THD for CHB_TTMC_PODSPWM

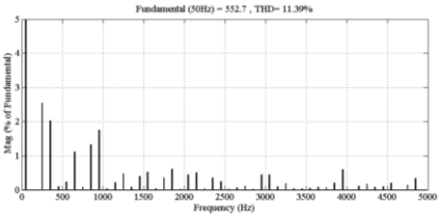

Figure 13. THD for CHB_TTMC_APODSPWM

The seven level CHBMLI we have done matlab simulation using Tripizodal tringular carrier based SVPWM techniques (TTMC-PDSVPWM, TTMC-PODSVPWM and TTMC-APODSVPWM). We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter show in Figure 14., Figure 15. And Figure 16. In the seven level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the TTMC-PDSVPWM techniques is perfect with the low THD, voltage and current shapes of the seven level CMLI. And we can observe the performance of THD is low in case TTMC based SVPWM comparision of TTMC based SPWM and trianular carrier based SPWM techniques.

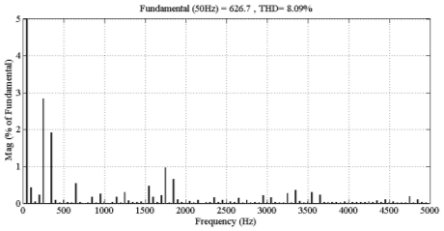

Figure 14. THD for CHB_TTMC_PDSVPWM

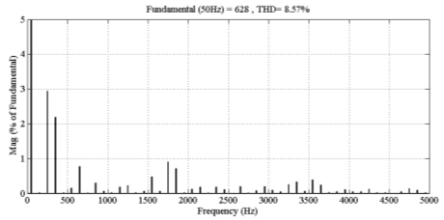

Figure 15. THD for CHB_TTMC_PODSVPWM

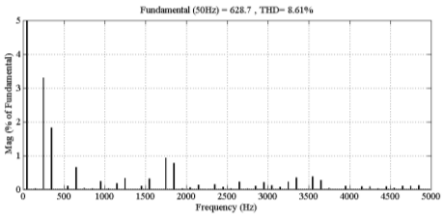

Figure 16. THD for CHB_TTMC_APODSVPWM

4.2. Diode Clamped Multilevel Inverter Simulation Results

The seven level NPCMLI we have done matlab simulation using SPWM techniques (PD-SPWM, POD-SPWM and APOD-SPWM). We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter show in Figure 17., Figure 18. And Figure 19. In the seven level single phase NPC inverter contain upper leg six switches and lower leg six switches with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the PD-SPWM techniques is perfect with the low THD, voltage and current shapes of the seven level NPCMLI.

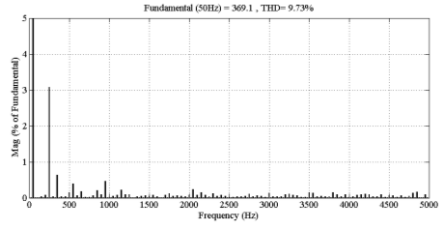

Figure 17. THD for NPC_PDSPWM

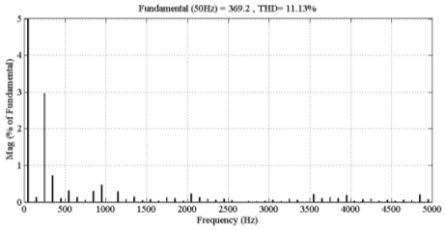

Figure 18. THD for NPC_PODSPWM

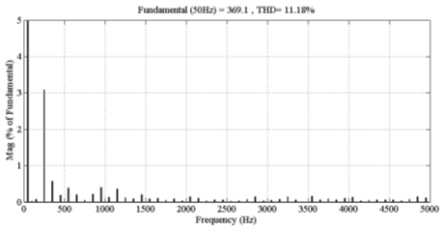

Figure 19. THD for NPC_APODSPWM

The seven level NPCMLI we have done matlab simulation using Tripizodal tringular carrier based SPWM techniques (TTMC-PDSPWM, TTMC-PODSPWM and TTMC-APODSPWM). We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter show in Figure 20., Figure 21. And Figure 22. In the seven level single phase NPC inverter contain upper leg six switches and lower leg six switches with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the TTMC-PDSPWM techniques is perfect with the low THD, voltage and current shapes of the seven level NPCMLI. And we can observe the performance of THD is low in case TTMC based SPWM comparision of trianular carrier based SPWM techniques.

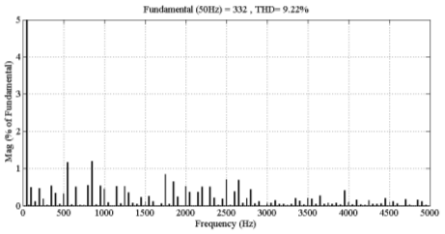

Figure 20. THD for NPC_TTMC_PDSPWM

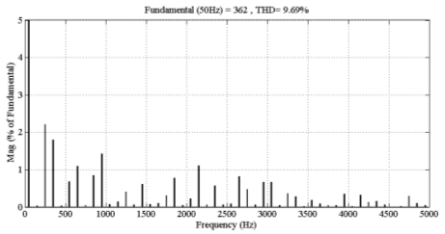

Figure 21. THD for NPC_TTMC_PODSPWM

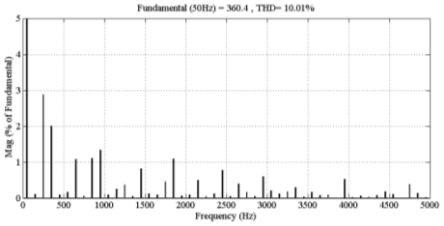

Figure 22. THD for NPC_TTMC_APODSPWM

The seven level NPCMLI we have done matlab simulation using Tripizodal tringular carrier based SVPWM techniques (TTMC-PDSVPWM, TTMC-PODSVPWM and TTMC-APODSVPWM). We have observe the performance of THD and load of the induction motor. The fft analysis of seven level inverter show in Figure 23, Figure 24 and Figure 25. In the seven level single phase NPC inverter contain upper leg six switches and lower leg six switches with the output phase voltage is 7 level and line voltage is 13 level of the inverter. We can observe the TTMC-PDSVPWM techniques is perfect with the low THD, voltage and current shapes of the seven level NPCMLI. And we can observe the performance of THD is low in case TTMC based SVPWM comparision of TTMC based SPWM and trianular carrier based SPWM techniques.

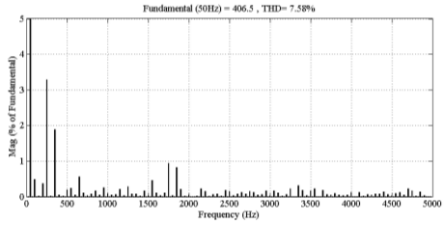

Figure 23. THD for NPC_TTMC_PDSVPWM

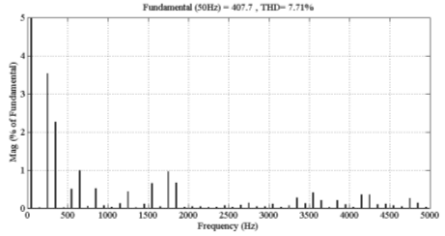

Figure 24. THD for NPC_TTMC_PODSVPWM

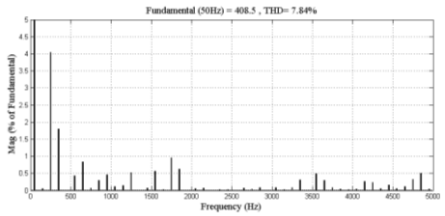

Figure 25. THD for NPC_TTMC_APODSVPWM

The seven level CMLI and NPC MLI was simulated with induction motor load, and the DC voltage given is 100V. In the seven level single phase CMLI contain three H-bridges with series connections with the output phase voltage is 7 level and line voltage is 13 level of the

inverter and NPC MLI witch contain upper six switches and lower six switches with the output phase voltage is 7 level and line voltage is 13 level of the inverter with perfect voltage and current shapes of the seven level CMLI and NPC MLI.

Table 1. Shown the comparision of THD for seven level CMLI and NPC inverters

PWM Techniques	CHBMLI (%THD)	NPCMLI(%THD)
PD-SPWM	10.81	9.73
POD-SPWM	12.20	11.13
APOD-SPWM	13.66	11.18
TTMC-PDPWM	10.58	9.22
TTMC-PODPWM	11.12	9.69
TTMC-APODPWM	11.39	10.01
TTMC-PDSVPWM	8.09	7.58
TTMC-PODSVPWM	8.57	7.71
TTMC-APODSVPWM	8.61	7.84

5. Conclusion

This paper focused on the performance and analysis trapezoidal triangular carrier has developed by adding triangular off set to sinusoidal fundamental waveform so as to shift the lower order harmonics to higher order side. This novel carrier is compared with the offset injected space vector reference waveform to generate the required PWM pulses to the inverter. To analyze the performance of the proposed PWM technique it is implemented on seven level cascaded and diode clamped Multi-level Inverter. The output line voltage of the NPCMLI slightly higher than the output line voltage of the cascaded multilevel inverters due to more losses avsilable in NPCMLI. However the THD of both multilevel inverters are reduced and comparision of THD for different PWM techniques along with both multilevel inverter.

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I also thank UGC for awarding me with RGNF FELLOWSHIP to carry out my research work (Ph.D).

Appendix

Table 2. System parameters of the induction motor

Parameters	Specifications
Input voltage	400VRMS(PhasePhase)
Inverter voltage	100(Volts)
Rotor speed	1440(RPM)
Fundamentalfrequency	50(Hz)
Switching frequency	1K(Hz)
Modulation index	1
Frequency modulation	200

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