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Forward Body Biased Low Power 4.0-10.6 GHz Wideband Low Noise Amplifier

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ABSTRACT

A forward body biased low power Low Noise Amplifier (LNA) is designed using Common Gate (CG) topology. By using current reuse technique between the first stage and second stage Common Source topology accompanied with forward body biasing leads to low power dissipation. A series to parallel tank circuit at this stage leads to wideband design. A shunt peaking inductor at the drain terminal of second stage causes the higher frequency peak to increase leading to wide bandwidth. Two CS cascade stages are used to increase the overall gain of the proposed LNA with a buffer stage at the output for output matching. The proposed LNA attained maximum gain of 26.39 dB with a gain greater than 16 dB over entire range. The circuit gives reflection coefficient less than – 10 dB with NF 2.7 dB. With V_dd of 0.925 V, a DC current of 8.32 mA is consumed giving 7.7 mW power consumption.

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1. INTRODUCTION

Wireless communication includes standards such as Global System for Mobile Communication (GSM), Code Division Multiple Access (CDMA), Wireless Local Area Network (WLAN), and Bluetooth which work in lower GHz frequency band. Earlier each application was developed using a single receiver. Now, instead of designing receiver for each individual application, transceiver design is focusing on integrated receiver which incorporates all these applications into a single device. RF front end design in the frequency range 3.1 – 10.6 GHz is an emerging research area for such high data rate wireless applications. This 7.5 GHz large bandwidth has the advantages of high data rate communication for continuous audio and video transmission, less multi-path fading and short distance communication useful for mobile communication, satellite communication and medical applications. These applications demand for low power dissipation, high gain, low Noise Figure (NF) and linearity. The first block of RF front end design after Band Pass Filter (BPF) is Low Noise Amplifier and is responsible for supporting such features. NF of the receiver is dependent on LNA. Sensitivity of receiver is dependent on gain (S_21) and NF, and linearity on reverse isolation (S_11) of LNA.

LNA design can be narrowband or wideband. It uses CMOS transistors in Common Source (CS) or Common Gate (CG) configuration [1]. CG topology is used for wideband design. CS topology can also be used for wideband design using some variations such as feedback (resistive, or reactive), or using a band pass filter prior to LNA block. For high gain and low NF, mainly CS topology is used.

Designing a wideband LNA requires complex derivations and analysis. In this paper, a wideband 4-10.6 GHz LNA is designed using CG configuration with forward body bias technique and multiple stages to boost the gain. Literature review is discussed in section 2. Section 3 states the proposed LNA circuit analysis

and design for input impedance, gain and NF with parameters affecting the design and their software implementation are explained. Section 4 gives results and discussion and compares the results obtained with earlier works and section 5 concludes the paper.

2. LITERATURE REVIEW

In radio receiver, the signal received from antenna is of very low value. To transfer it to output section, it needs to be amplified. Using maximum power transfer theorem, amplification is achieved when the input interface of LNA is matched with the resistance of antenna. Several topologies have been discussed with variations to achieve input matching and maximum transfer of power from antenna to output. Wideband LNAs can be designed using various techniques. Most common are [2]: 1) CS with resistive termination, 2) CS topology with resistive or reactive feedback, 3) CS with input filter, 4) CG topology, and 5) distributed amplifiers.

The easiest way to design LNA is by placing a shunt resistor at CS CMOS input section [3]. This resistance is matched with antenna resistance of 50 Ω. Main drawback is the attenuation of signal by shunt resistor and inclusion of thermal noise, which leads to highly unacceptable NF. A number of literatures are dedicated to using resistive [6] or reactive feedback [9]. A wideband LNA consisting of resistive feedback and a band pass filter at the input section is designed [4]. The resistive feedback provides the stability to the system and also decreases the overall NF of the circuit. Third order Chebyshev band pass filter is used to provide input matching and wide bandwidth. A 2.4 GHz narrowband LNA with shunt resistive feedback in Common source topology is designed with an inter-stage inductor for better reverse isolation (S_{12}), low NF and good stability [5]. Resistive feedback first stage is used for wideband operation with good input return loss, but noise introduced by the resistor increases the NF [7]. To reduce the NF, noise cancelling source follower feedback technique is used. In [8], a wideband LNA is designed with transformer reactive feedback from drain to gate terminal. It contributes less noise by eliminating the transconductance (g_m) degradation occurring due to source degeneration.

Filter LNAs provide easy input matching with wideband operation. Generally a band pass filter [10] is used at the input section between antenna and LNA. This consists of passive elements in the form of inductors and capacitors used in T or Π configurations. A CG followed by CS stage is used to design LNA [11]. First stage provides a good input impedance matching with wideband operation. A single to differential converter LNA is designed for noise and distortion cancellation. Better NF is achieved at the cost of high-power consumption. A CS inductive source degeneration inductor with a passive notch filter LNA is designed in [12]. The passive notch filter acts as a 3rd order harmonic rejection filter and also enhances the impedance matching performance of the designed LNA. It helps in desensitizing the blockers at the starting point of the receiver.

Distributed amplifier LNA is also popular for reducing the noise by cancellation. A distributed LNA at 40 GHz is designed and NF is decreased by tapering the gate and drain terminals of transistors and transmission lines [13]. Increasing the tapering factor leads to increase in characteristic impedance which leads to high gain, but it results in degraded NF. NF can be improved by decreasing the tapering, so it results in a trade-off for gain and NF.

Two low power UWB LNAs with common source and common gate architectures respectively are demonstrated in [14]. The technique of using reused current reduces power. The suggested circuit uses an output buffer that is used by a common source amplifier with shunt-shunt feedback to increase gain and reduce noise. A 3.1–10.6 GHz UWB low noise amplifier (LNA) with low power and high gain is presented in [15]. A parallel LC load and resistive shunt feedback architecture are used in the UWB LNA's first stage to simultaneously achieve wideband input matching and low noise figure. The second stage uses the forward body bias approach and improved current reused cascade structure to function at lower supply voltages and with less power consumption. A self-body biased common-gate (CG) configuration low noise amplifier (LNA) is proposed [16]. Using a 90 nm CMOS process, the suggested LNA is made for ultra-wideband (UWB) frequencies between 3 and 14 GHz. Wide-band input matching with a low Noise Figure (NF) for the UWB frequency has been achieved at the input stage using a common gate arrangement with self-body biasing. Between common-gate and cascaded common source (CS) stages, a parallel to series RLC network has been employed as an impedance matching network. It can achieve an output reflection coefficient of less than -10.8 dB by using a buffer stage at the output.

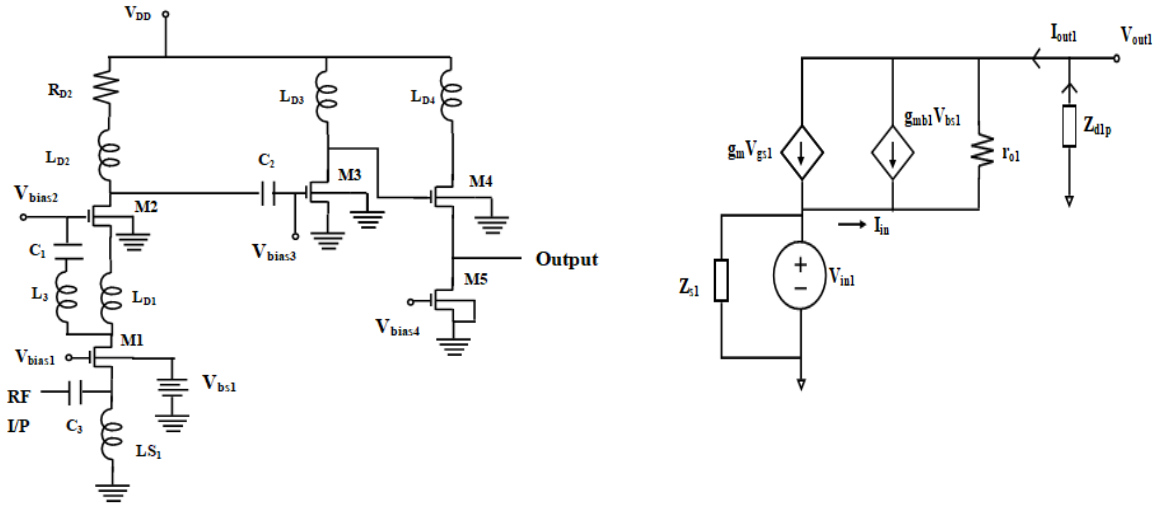
To enhance radio frequency (RF) performance, a wideband Low-Noise Amplifier (LNA) that employs a two-stage cascade arrangement is proposed in [17]. The suggested LNA offers wideband input matching using a common gate (CG) input stage and wideband gain response was made feasible by inserting peaking inductors at each stage's drain terminals. Cadence Spectre-RF is used to design and simulate CG current-reused UWB LNA using a 90 nm CMOS technology [18]. A common gate input stage, a cascoded common-source current-reused stage, and an output matching circuit make up the proposed LNA design.

Using 180 nm PTM node, a three stage UWB LNA is designed using CG input stage, followed by CS topology and an output source follower stage [19]. Second stage consists of peaking inductor which provides an impedance component which increases the bandwidth and keeps the impedance in the region constant. Low power consumption is obtained by using Forward Body Bias (FBB) technique. FBB helps in reducing the supply voltage which results in low power consumption. A 90 nm CMOS-based low-power LNA at 0.1–20 GHz is described in [20]. It is intended to use unique self-biased resistive feedback architecture. Two CS stages are used for high gain. The feedback loop's two internal inductors as well as a shunt-peaking inductor are used to increase the bandwidth. A novel low-voltage, low-power noise-cancelling technique based on balanced loads, local feedback g_m-boosting, and 65 nm CMOS is proposed [21]. The amount of loop gain used by local feedback to increase the CG stage's overall g_m can reduce supply voltage and current consumption needs. To reduce the gain and phase mismatches at the differential output, the cross-coupled cascode stage functions as a differential current balancer.

As discussed in literature review, wideband designs typically use CG topology. The most common topology for high gain and low NF is CS. In comparison to CS architecture, a Common Gate amplifier has a greater NF value and a lower power gain. Even then, it has already shown itself to be a strong contender for creating wideband low NF amplifiers. It provides wideband input matching by making it equal to $1/g_m$. Also, low NF can be obtained by using an inductive degeneration inductor (L_s) at the source terminal of CG stage. Along with low NF and wideband input matching higher gain can be achieved by using multiple stages of CS topology after CG stage. Another factor emphasized in literature is use of low power designs. Various techniques include current reuse methods or using forward body bias techniques. In this research paper both these concepts are incorporated in the design for low power architecture. Current reuse includes using a series to parallel matching between the stages. This not only reduces the overall power of the design but also increases the bandwidth to a larger extent.

3. PROPOSED LNA CIRCUIT ANALYSIS AND DESIGN

Using a 90 nm CMOS PTM node, the LNA proposed here consists of four phases. The suggested UWB LNA's circuit schematic is shown in fig. 1 (a). It consists of a common gate (CG) stage for wideband input matching, two common source (CS) amplifier stages and a source follower as the output buffer. First, the CG input phase has an inductor, designated as L_{s1}, a MOSFET M1, and a drain inductor L_{d1}. A lower Q value is achieved by setting the inductor L_{s1} to block any input signal loss through it. Through the resonance of the M1's gate-to-source capacitance (C_{gs1}), it creates a parallel tank circuit which resonates at a particular narrowband frequency. At this frequency, the input impedance of the first stage is equal to transconductance ($1/g_m$) and hence leads to wideband input matching. Both power and noise matching are objectives of this input matching. Transistor M1's width is set to maintain a compromise between noise figure, power gain, input reflection coefficient, and power consumption, as the common gate stage of the LNA is the one that consumes the most power. M1 uses the Forward Body Bias (FBB) method in the CG input stage. By lowering M1 threshold voltage (V_T), this FBB approach permits ultra-low voltage design. The power consumption from supply voltage (V_{dd}) can be successfully decreased in this way.



(a) (b)

Figure 1. (a) Proposed LNA Circuit; (b) Small Signal Equivalent Circuit

A parallel to series LC network has been employed between the common gate first stage and the following common source stage to ensure the maximum power flow from stage one to succeeding stages. In this, the drain inductor L_{d1} creates a parallel tank that resonates with the transistor M1's gate-to-drain parasitic capacitance C_{gd1} at $1/\sqrt{(L_{d1}C_{gd1})}$, while L_3 creates a series LC tank with input capacitance (C_1) and the MOSFET M2's gate-to-source parasitic capacitance (C_{gs2}). A frequency response resembling a band-pass filter can be created by appropriately choosing the inductors and capacitors in parallel and series tank circuits to resonate at the identical resonance frequency and by preserving $L_{d1}C_{gd1} = L_3C_1$. Third phase is again a CS topology and is used to further enhance the power gain of the circuit. The final step is a source follower buffer, which includes the MOSFETs M4 and M5 in common drain topology and offers an output matching network to achieve output impedance of 50 Ω over a broad bandwidth.

3.1. Common Gate Stage Input Matching Analysis

Input matching is done by finding the input impedance. If only the CG stage is considered, then L_{s1} and M1's parasitic capacitance (C_{gs1}) and g_{m1} are used to achieve input matching to 50 Ω. The calculation is shown in equation 1 and when $w = 1/\sqrt{(L_{s1}C_{gs1})}$, imaginary part is zero and Z_{in} is simply equal to $1/g_{m1}$.

$$Z_{in} = \frac{1}{g_{m1}+sC_{gs1}+\frac{1}{sL_{s1}}} = \frac{jwL_{s1}(1-w^2C_{gs1}L_{s1})+(wL_{s1})^2g_{m1}}{(1-w^2C_{gs1}L_{s1})^2+(wL_{s1})^2(g_{m1})^2} \quad (1)$$

For the complete analysis of input impedance, circuit includes the input section and output impedance of first stage. The small signal equivalent circuit is shown in fig. 1 (b). The effect of input capacitance C_3 is ignored and kept open circuit. Input impedance considering the effect of transconductance of source body bias (g_{mb1}) is calculated and expressed as follows:

$$Z_{in} = \frac{\{r_{o1} + (g_{mb1} * r_{o1} + 1)Z_{d1p}\}}{\{1 + (g_{m1} + g_{mb1})r_{o1}\}} // Z_{s1} \quad (2)$$

$$where\ Z_{s1} = SL_{s1} || \frac{1}{SC_{gs1}} \quad (3)$$

$$and\ Z_{d1p} = (SL_{D1} || \frac{1}{SC_{gd1}}) \ ||(SL_3 + \frac{1}{SC_1}) \quad (4)$$

Assuming $r_{o1} >>> Z_{d1P}$, and g_{mb1} is neglected, and then $Z_{in}$is equal to $1/g_{m1}$. Z_{s1} is the total impedance at the source and Z_{d1P} is the total impedance at the drain of the CG stage. The input impedance is also used to find out input reflection coefficient (S_{11}) given by:

$$S_{11} = \frac{Z_{in} - R_s}{Z_{in} + R_s} \quad (5)$$

Input reflection coefficient depends on Z_{d1P} and g_{m1}. By varying these factors, good input reflection coefficient can be obtained.

3.2. Voltage Gain (A_v)

The frequency response of the complete LNA circuit can be obtained by analyzing each individual stage gain. The first stage of CG topology has low gain and to increase the total gain multiple stages of CS are cascaded with the CG stage. The gain of first stage is:

$$A_{v1} = \frac{V_{out1}}{V_{in1}} = \frac{(1 + (g_{m1} + g_{mb1}) * r_{o1})Z_{d1p}}{(1 + g_{mb1}r_{o1})Z_{d1p} + r_{o1}} \cong \frac{g_{m1} * r_{o1}}{1 + \frac{r_{o1}}{Z_{d1p}}} \cong g_{m1}Z_{d1p} \quad (6)$$

Drain inductance (L_{d2}) and resistance (R_{d2}) are adopted in the design of the second stage CS amplifier to achieve adequate gain over the wide band and establish the LNA's 3-dB bandwidth. The L_{d2} extends the useable bandwidth and increases amplification at higher frequencies. The impedance component $SL_{d2}g_{m2}$ is introduced into the gain function A_{v2} with L_{d2} for shunt peaking, which can enhance A_{v2} with rising frequency and counteract the degeneration from $SR_{d2}C$ to keep the overall impedance virtually constant over a wider bandwidth. Here C shows the load capacitance acting at the output of common source second phase. To achieve high gain, inductor L_{d2} must be optimized, and it must be sufficiently low to maintain the resonance frequency, $w = 1/\sqrt{L_{d2}\ C}$.

$$A_{v2} = -g_{m2}\left\{(R_{D2} + sL_{D2})// \frac{1}{sC}\right\} = -\frac{g_{m2}R_{D2} + sL_{D2}g_{m2}}{1 + sR_{D2}C + s^2L_{D2}C} \quad (7)$$

The gain of the third phase and the total gain respectively are given as:

$$A_{v3} = -g_{m3}((r_{o3} + sL_{D3}) // \frac{1}{sC_{gd3}}) \quad (8)$$

$$A_v = A_{v1} * A_{v2} * A_{v3} \quad (9)$$

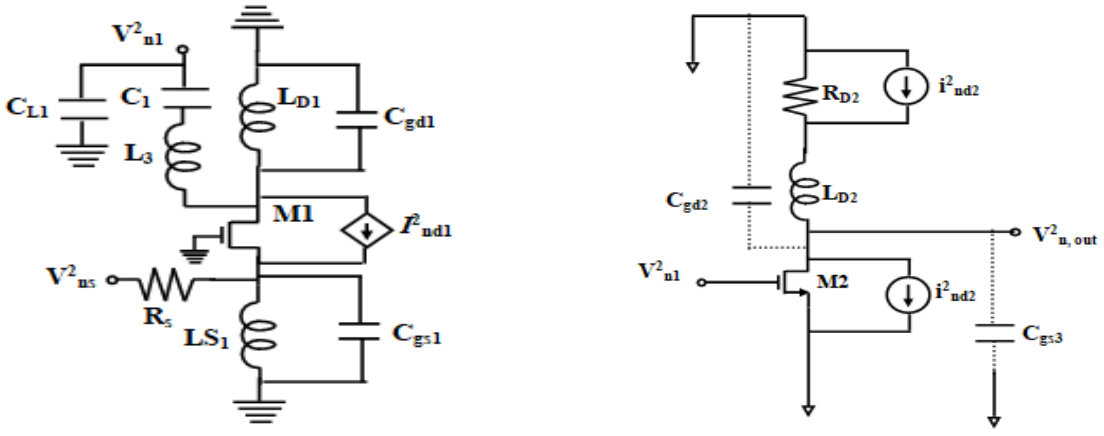
3.3. Noise Figure Analysis

Noise figure affects the detection accuracy at the output. Noise can be thermal noise which is due to random motion of electrons. The sources of this noise are channel and gate contacts of a MOS device, resistors and conducting metal contacts. Another component of noise is flicker noise where electron flow is disturbed by trapping and release of charge carriers. In MOS device any defect in oxide layer is a potential candidate for the trapping.

Friis formula is used to find out the total noise factor (F) of a cascade of stages where each stage has its own power gain and noise factor. According to the formula the noise factor of succeeding stages gets decreased by the gain multiplication up to that stage. As the gain of CS stages is very high, so, later stages have negligible impact on the total noise factor. Considering this fact, the NF analysis is carried out on first two stages only. In the proposed LNA due to the use of CG first phase due care should be given to evaluate the noise parameters, as this stage is noisier than narrowband LNA using source degeneration. To optimize the NF analysis, noise power due to inductors and capacitors are assumed to be negligible in comparison to MOSFETs and resistors. Also flicker noise can be ignored at GHz frequency band range. So its effect is not evaluated. The noise sources for the first stage includes mean square noise voltage $V_{ns}^2 = 4KTR_s\Delta f$ of source resistance R_s, and mean square noise current due to MOSFET1 ($i_{nd1}^2 = 4KT\gamma g_{m1}\Delta f$). Noise sources of second stage includes mean square noise current due to MOSFET2 ($i_{nd2}^2 = 4KT\gamma g_{m2}\Delta f$) and mean square noise current of drain resistance R_{d2} of second stage ($i_n^2 R_{d2} = \frac{4KT\Delta f}{R_{d2}}$). Here K, T, Δf and γ represents the Boltzmann's coefficient, absolute temperature in Kelvin, noise bandwidth in HZ and thermal noise coefficient ranging from 1-2 for short channel devices in saturation mode. The mean square noise voltage of first stage also gets amplified by second stage and acts as an important factor if calculating the overall NF of the proposed LNA. The noise factor (F) of LNA circuit is given as:

$$F = \frac{V_{n,out}^2}{A_v^2} * \frac{1}{V_{ns}^2} \quad (10)$$

$V_{n,out}^2$, and A_v, shows the total noise at stage 2 output, and the overall gain of both stages respectively. The noise equivalent circuit of CG stage is as shown in fig. 2 (a). Noise bandwidth is assumed to be 1 Hz. As the noise sources are deemed to be un-correlated, the total output mean square noise voltage is due to both source resistance and MOSFET1 channel induced mean square noise current in terms of noise voltage. Noise power due to source resistance is also amplified by the first stage, so its impact on output is evaluated by using the gain of this stage.



(a) (b)

Figure 2. (a) Noise Sources of First Stage (b) Noise Sources of Second stage

To find out the mean square noise voltage due to MOSFET1 ($V_{n1\_M1}^2$), impedance at drain terminal consisting of Z_{d1p}, Z_3 and C_{L1} (parasitic gate-source capacitance of 2nd stage and parasitic gate-drain capacitance of 2nd stage using Miller effect) are required. The noise voltage can be expressed as:

$$V_{n1\_M1}^2 = (\frac{Z_{d1p}}{1 + sC_{L1}Z_3})^2 * I_{nd1}^2 \quad (11)$$

$$where\ Z_3 = SL_3 + \frac{1}{SC}\ and\ C_{L1} = C_{gs2} + C_{gd2} \quad (12)$$

Considering V_{n1}^2, I_{nd2}^2, and I_{nRd2}^2 as noise sources for second stage NF analysis (fig. 2 (b)), the total noise power at the output of second stage is as follows:

$$V_{n\_2nd}^2 = (\frac{Z_{D2}}{1 + SC_{gs3}})^2 * \{I_{nd2}^2 + \frac{V_{nR}^2}{(R_{D2} + SL_{D2})^2}\} \quad (13)$$

$$where\ V_{nR}^2 = 4KTR_{D2}\ and\ Z_{D2} = (R_{D2} + SL_{D2})\ //\ \frac{1}{sC_{gd2}} \quad (14)$$

Putting values of $V_{n,out}^2$, V_{ns}^2, and A_v derived for finding out the noise factor (F), the approximately calculated formula is obtained as:

$$F = 1 + \frac{1}{A_{v1}^2 * R_S} * \left\{(\frac{Z_{d1p}}{1 + sC_{L1}Z_3})^2 \gamma g_{m1} + \frac{\gamma}{g_{m2}} + \frac{R_{D2}}{{g_{m2}}^2 * (R_{D2} + SL_3)}\right\} \quad (15)$$

Based on above equation, it can be deduced that the noise factor is inversely proportional to g_{m1} of MOSFET1 and proportional to load impedance of first stage. To achieve low F, and lower power consumption, g_{m1} should be made high. But this leads to low gain. To attain both low F and high gain g_{m2} of M2 should be high. Increase in g_{m2} causes more power dissipation, so there is a need to optimize g_{m1} and g_{m2} which can be done by optimizing MOSFETs width.

3.4. Power Reduction Techniques

3.4.1. Forward Body Biasing

Wideband input and output impedance matching, a feature of the Distributed Amplifier (DA), has made it a popular choice for wideband design. The main disadvantage of DA however, seems to be its high-power consumption. The UWB LNA uses FBB as a reduced voltage and minimal power design improvement [15]. For low voltage operations use of multiple numbers of transistors (M1-M5) is not good. Forward body bias approach is used to drive the UWB LNA to mitigate the restrictions placed on the supply voltage. By using the forward body bias technique, the threshold voltage of the transistor M1 can be decreased, negating the requirement for the higher supply voltage used in standard LNAs with the same amount of current [16], [19]. The lower V_{dd} coupled with lower threshold voltage (V_T) led by FBB is the operational concept. Power reduction may result from the efficient reduction of V_{dd}. FBB is used here in the first CG stage. The threshold voltage of the MOSFET is given as:

$$V_t = V_{t0} + \gamma[\sqrt{2\varphi_f - V_{sb}} - \sqrt{2\varphi_f} \quad (16)$$

Here V_{t0}, γ, φ_f represents threshold voltage for V_{sb} =0, fabrication process parameter and semiconductor physical parameter in the range of 0.3-0.4 respectively. It has been noted that a gradual shift in the body-to-source voltage results in a reduction in threshold voltage. As a result, a gate-to-source voltage of the transistor M1 that is substantially lower than that of the standard cascade stage is practicable. Due to this, the suggested current reused cascade stage's supply voltage can be designed to be lower than that of the conventional cascade stage. The transistor M1 may function at reduced supply voltages and power requirements while maintaining the same device features in aspects of gain, linearity, and NF.

3.4.2. Current Reuse

The common gate amplifier is the initial phase of proposed LNA. The first stage's driving current does not need to be adjusted because the second stage is cascaded onto it, reducing the overall power consumption of the UWB LNA. Due to the small voltage drop across the load inductors L_{d1} and L_{d2} of the first and second stages, respectively, a low supply voltage is made achievable.

3.5. Stability

It measures the tendency of LNA to oscillate. Two port networks are characterized by their scattering (S) parameters. It allows the calculation of potential instabilities. A 2-port network is unconditionally stable if its reflection coefficients Γ_{in} and Γ_{out} have magnitude less than 1 and impedances seen from the input and output have positive real parts and are independent of load impedances at input and

output. LNA instability is due to insufficient RF isolation between supply lines of successive amplifier stages that provide positive feedback. Excessive parasitic inductance on ground connections and too much in-band and out-of-band gain are also some reasons for instability. The stability factor (K) is given as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 * |S_{12}S_{21}|} > 1 \quad (17)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (18)$$

When $|S_{22}| < 1$ and $|S_{11}| < 1$, the LNA is unconditionally stable for any combination of source and load impedance. If K < 1 and Δ > 1, the source and load impedance must be carefully chosen.

4. RESULTS AND DISCUSSION

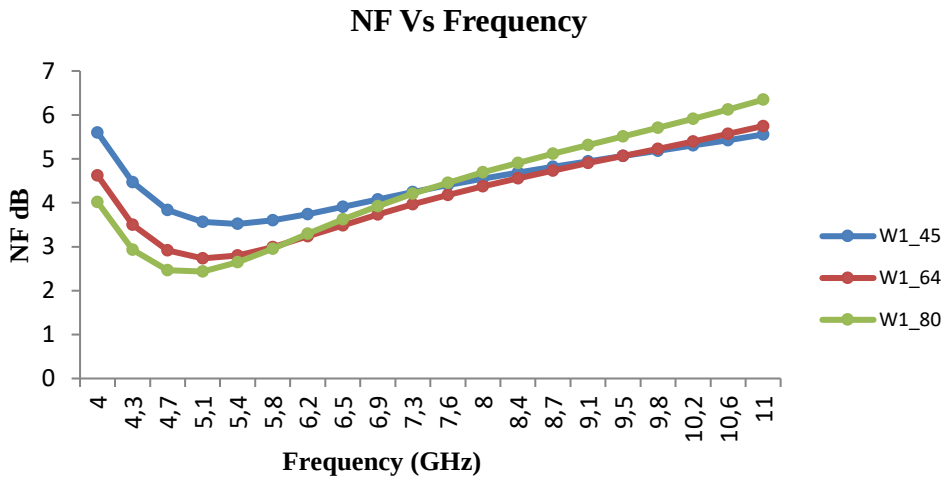
Using 90 nm PTM node CMOS, the proposed LNA circuit is implemented in ADS and simulated for the parameters discussed above. The biasing resistors R_1-R_4 are not shown in circuit diagram for circuit simplification. The component values of the proposed circuit used are:

Table 1. Proposed Circuit Component Values

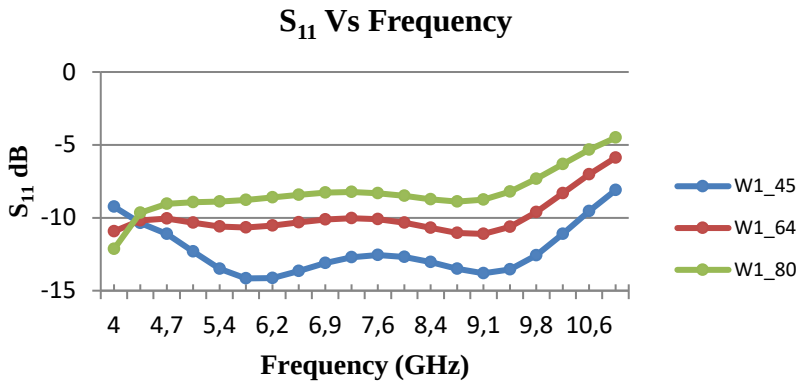
Transistor {W (µm)*L (nm)}	Inductance (nH)	Capacitance (pF)	Voltage (Volts)	Resistance (Ω)
M1 64.1 * 90	L_{s1} 3.8	C_1 2.2	V_{bias1} 0.36	R_1 4.4 K
M2 36.3 * 90	L_{D1} 5.01	C_2 19	V_{bias2} 0.65	R_2 9 K
M3 55 * 90	L_3 4.37	C_3 0.4	V_{bias3} 0.36	R_3 5.5 K
M4 8 * 90	L_{D2} 9		V_{bias4} 0.9	R_4 2 K
M5 1 * 90	L_{D3} 1.96		V_{bs} 0.45	R_{D2} 15
	L_{D4} 1.7			

4.1. Effect of Width (W1) of MOS1 on Noise Figure, S11 of Proposed LNA

For determining NF, first stage of proposed LNA, i.e. CG topology is of prime importance. First the effect of width (W_1) of MOS1 is examined. Width of a MOS is a prime parameter to determine g_{m1}. Analysis of NF shows that when the transconductance of MOS increases NF decreases. The effect is shown in fig. 3 (a). As shown, as the width of MOS1 is increased NF decreases. This is in accordance with the equation of NF described earlier. Along with NF, input reflection coefficient (S_{11}) is mainly dependent on the performance of CG phase. It depends on the input impedance of this topology. As shown in fig. 3 (b), as the width of MOS1 increases the input reflection coefficient becomes worse. Input impedance is approximated to be equal to $1/g_{m1}$ and as the width increases, g_{m1} also increases which results in decrease in Z_{in} and hence S_{11}.



(a)

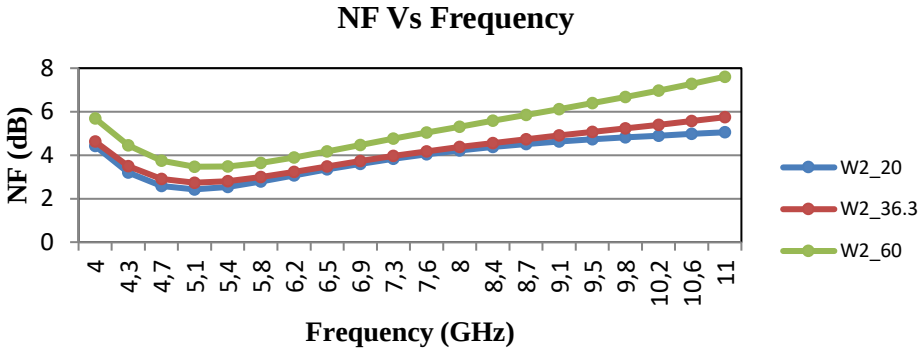


(b)

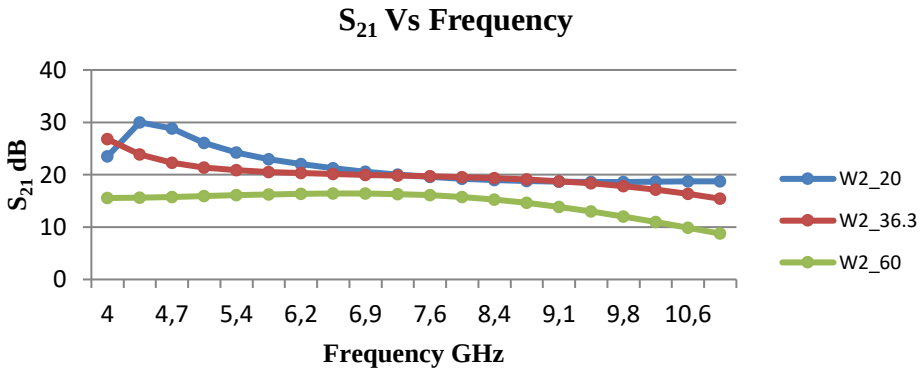
Figure 3. (a) Effect of W_1 on Noise Figure and (b) Input Reflection Coefficient

4.2. Effect of Width (W_2, W_3) of MOS2 and MOS3 on NF and Gain (S_21)

The effect of W_2 on NF and S_{21} are shown in fig. 4 (a) and (b) respectively. In NF analysis, first two stages are affecting the overall NF. As W_2 increases NF also increases as the effect of input impedance of second stage impacts the load impedance of first stage and hence the NF of the complete circuit. Most of the gain of the proposed LNA is accommodated by second and third stage CS phases. With increase in W_2 the gain of proposed LNA decreases and after certain limit it starts decreasing more with a small increase in the width. It occurs due to shunt series matching circuit used at the input of second stage. The impact of $\boldsymbol{W_3}$ is also checked in simulations. The simulations clearly show that the overall gain of the circuit increases with increase in the width of third stage and there is negligible impact on NF. In our analysis of NF, it was stated that first two stages are the dominant factors for increase in NF and after that due to Friis formula gain terms multiplication occur in the denominator and as the stages increases the overall impact of higher stages NF is negligible on total NF of complete circuit.



(a)

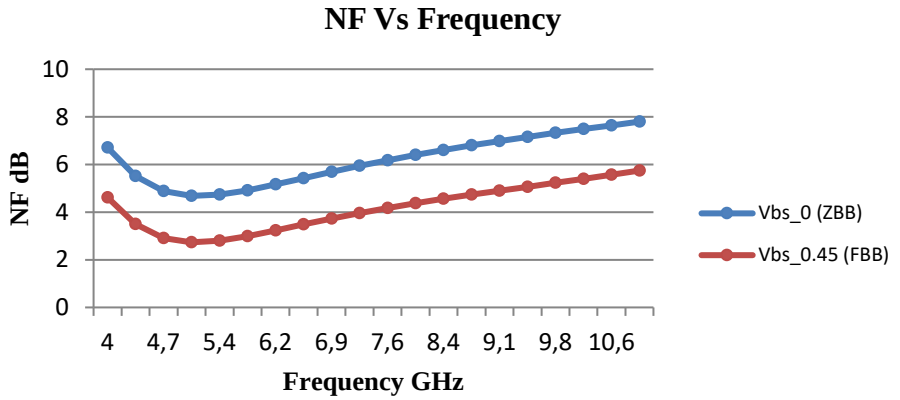


(b)

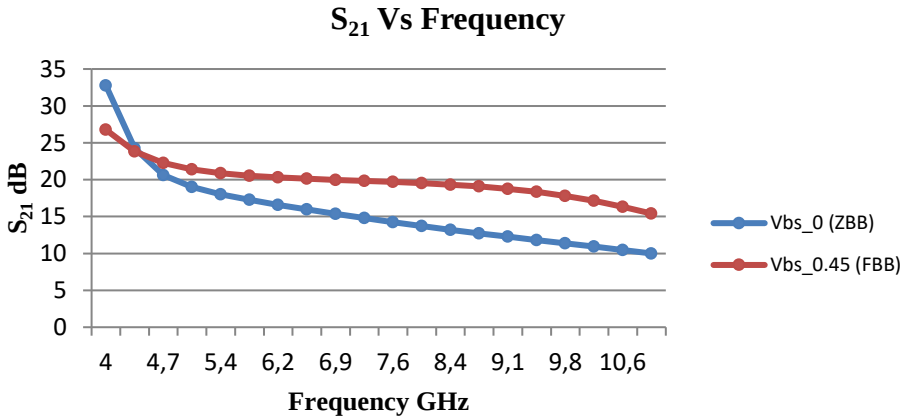
Figure 4. (a) Effect of W_2on Noise Figure and (b) Gain (S_{21})

4.3. Effect of Source-Body Voltage (V_bs) on NF and S_21

Figure 5 (a) and (b) shows the simulation results of variation of NF and S_{21} with frequency for changes in source-body voltage (V_{bs}) respectively. Here Zero Body Bias (ZBB) and Forward Body Bias (FBB) represent the 0 V and 0.45 V respectively applied to body terminal of M1. As shown in figures, FBB improves the gain, lowers NF in comparison to ZBB. With same supply voltage of 0.925 V, ZBB provides 13.92 mA of dc current leading to 12.87 mW of power consumption while with FBB dc current is 8.32 mA which results into a power consumption of only 7.7 mW.



(a)

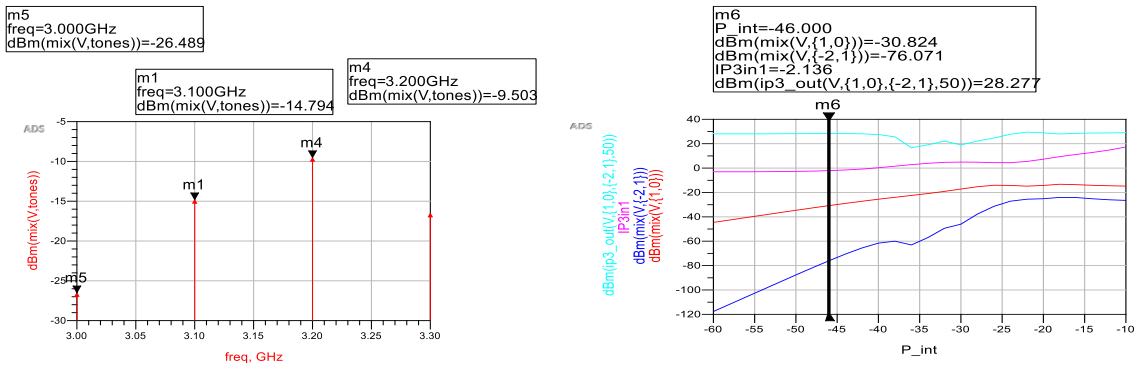


(b)

Figure 5. (a) Effect of V_{bs} on Noise Figure and (b) S_{21}

4.4. Input Intercept Point (IIP3) and Output Intercept Point (OIP3)

IIP3 is a way to quantify Inter-Modulation Distortion (IMD) and by extension the linearity of device under test. Two signals closely spaced in frequency and equal in amplitude drive a non-linear circuit generating new unwanted harmonics. A device is said to be linear if the output is directly proportional to input of device. After a certain level, the output becomes non-linear. Harmonics are copies of a signal appearing at integer multiples of two fundamental signals. Inter-modulation occurs when two or more signals mix in a non-linear device. If f_1 and f_2 are two fundamental frequencies, then $2f_1$-$f_2$and $2f_2$-f_1 are the third order inter-modulation product terms. When the frequencies are very close to the fundamental signals it is difficult to filter them. These lead to IIP3 and OIP3. For every 1 dB increase in fundamental signals 3rd order IMD products increases by 3 dB. To show the impact of non-linear behavior of LNA and to specify the range up to which the device works in linear region, two single tone signals at frequencies of 3.1 GHz and 3.2 GHz are used and it produces 3rd order harmonics at 3 GHz and 3.3 GHz shown in fig. 6 (a). Then IIP3 and OIP3 are simulated for the region up to where the device is in linear region. Figure 6 (b) shows the curve containing the fundamental signal at 3.1 GHz, the IMD term at 3 GHz and corresponding IIP3 and OIP3 curves. Firstly the slope of the 3 GHz signal is taken, and the power point is considered where the graph is having constant slope. Now based on the power at that point a marker is set and the value of IIP3 and OIP3 are noted (fig. 6 (b)). The proposed LNA has an IIP3 of -2.136 dBm and an OIP3 of 28.277 dBm. After these points the proposed circuit behaves in a non-linear manner.

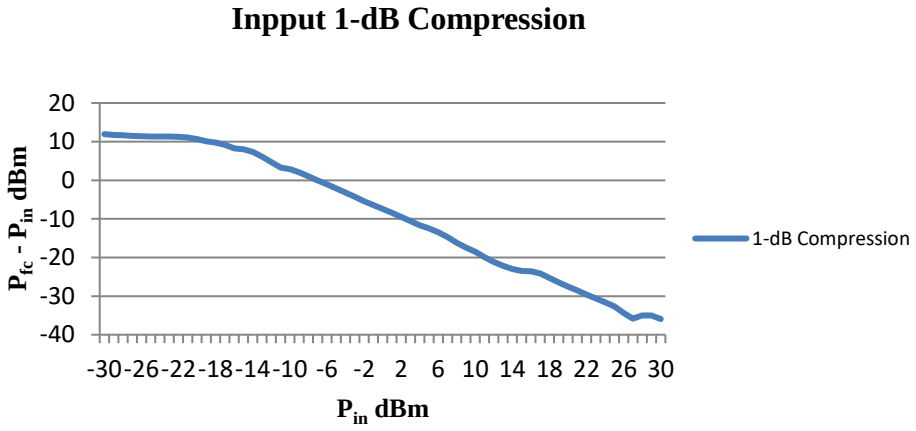


(a) (b)

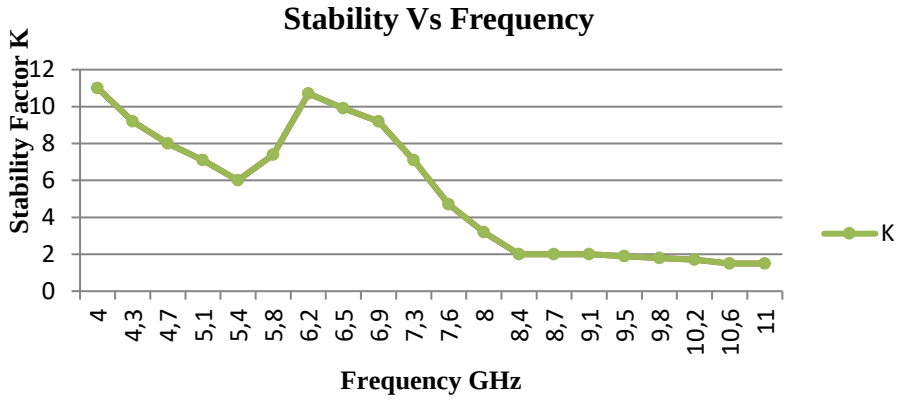
Figure 6. (a) Output Voltage with IMD Points and (b) IIP3 and OIP3 Curve

4.5. Input and Output 1-dB Compression Point

An amplifier provides a constant gain over a specific frequency range. In dB, the gain is equal to output power minus input power in dB. The 1-dB compression point (P1dB) is the output power level at which the gain decreases 1 dB from its constant value. Once an amplifier reaches its P1dB it goes into compression and becomes a non-linear device, producing distortion, harmonics, and inter-modulation products. Up to this point the LNA operates linearly. To find out 1 dB compression point, harmonic balance simulation is done in ADS to find out the output power (P_{fc}) in terms of input power (P_{in}). Then to find out 1-dB compression gain ($P_{fc} - P_{in}$) is plotted with respect to P_{in} and from maximum gain 1-dB point is taken. Here maximum gain is 11.937 dBm, so 10.937 dBm is the 1 dB compression point (fig. 7 (a)). At 10.937 dBm, P_{in} is -21dB and P_{fc} is -9.958 dB which gives the output 1-dB compression point.



(a)



(b)

Figure 7. (a) Input 1-dB Compression Point and (b) Stability Factor Vs Frequency

4.6. Stability

Another important parameter is the stability. As discussed above, for stability the value of K should be greater than 1. As shown in fig. 7 (b), the value of K is greater than 1 for the complete range of interest which illustrates the unconditional stability of the proposed LNA circuit.

The proposed circuit is compared with earlier research works and is presented in table 2. The topology of first stage, techniques used with frequency range, S-parameters, NF, power consumption and IIP3 of earlier works are summarized along with the proposed work. The results clearly demonstrate that excellent performance in terms of gain, NF, power consumption, and IIP3 is attained with reasonable reflection coefficient over the entire range. The proposed LNA attained maximum gain of 26.39 dB with a gain greater than 16 dB over entire range. With supply voltage of 0.925 V the proposed LNA achieved very low power consumption of 7.7 mW. FBB and current reuse techniques helped in reducing the power consumption.

Table 2. Performance Comparison of Proposed Work with Earlier Works

	[9]	[15]	[16]	[17]	[18]	[19]	[20]	This Work
PTM Node (nm)	32	180	90	180	90	180	90	90
Frequency (GHz)	3.1-10.6	3.1-10.6	3-14	8.5-20	3.1-10.6	2-10	0.1-20	4-10.6
Topology	CS	CS	CG	CG	CG	CG	CS	CG
Technique	Current reuse, inductive peaking	FBB, Current Reuse, resistive feedback	Self-body biased	Peaking Inductors	Current Reuse	FBB	Peaking Inductor, self-biased feedback R	FBB, Current Reuse, Peaking Inductor
Gain (S_{21}) dB	23.8	14.4	15.9	11.13	19.2-20.8	> 10	12.7	> 16
Reflection Coefficient (S_{11}) dB	< - 7.5	< - 10.6	< -10.2	< - 9.44	< - 10.6	< - 14	< -10	< -10
NF (dB)	2.7	2.2-3.2	1.68	2.19-3.23	2.3-3.7	2.83-4.7	3.3	2.7
Power Consumption (mW)	8.05 @ 0.7 V	9 @ 1.5 V	20.1 @ 1.2 V	5.4 @ 1 V	5.05 @ 0.7 V	4.2 @ 0.85 V	12.6 @ 1.2 V	7.7 @ 0.925 V
IIP3 (dBm)	-10	-6	-8	0.96	-8	4.2	-1	-2.136
P1dB (dBm)	-20	-15.5	-13	-	-17	-	-	10.937

5. CONCLUSION

A wideband 4-10.6 GHz low power low noise LNA is designed using CG first phase followed by two stages of CS topology and a final buffer stage for good output matching. As the gain of first stage is less so to improve the overall gain two CS stages provide high gain with a maximum of 26.39 dB with greater than 16 dB in the complete range considered. The work focuses on reducing the power consumption to increase the battery life of devices. For this forward body bias technique at first stage followed by current reuse method in the second stage input are used. This led to a power consumption of only 7.7 mW with a supply voltage of 0.925 V. The proposed LNA is designed using 90 nm PTM node and provided a minimum NF of 2.7 dB with acceptable NF over the entire range. The circuit is stable and provides linear behavior to a larger extent. The IIP3 attained is -2.136 dBm with one dB compression point of 10.937 dBm.

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