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Performance Evaluation of Advanced PLL Techniques For Accurate FFPS Component Extraction

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ABSTRACT

It is very necessary to adopt fundamental frequency positive sequence (FFPS) element extraction methods in order to maximise the efficiency of integrating and handling the use of renewable energy sources (RES). The decision to act in this manner is made with the purpose of contributing to the accomplishment of the aforementioned aim. The capability of the synchronous references frame phase-locked loop to reject variations over a broad variety of grid conditions is enhanced as a result of this. This is particularly true for voltage sags and surges that are accompanied by harmonics, irrespective of whether the harmonics are the result of balanced or unbalanced electrical current fluctuations. The accuracy of the extraction of FFPS components is significantly influenced by the frequency deviation in SRF-PLL systems. The frequency deviation is another critical component. This is a result of the frequency deviation not remaining constant. An investigation is being conducted to ascertain the effectiveness of a various advanced PLL techniques, such as the cascaded delayed signal cancellation (CDSC), the dual second-order generalized integrator (DSOGI) and the multiple delayed signal cancellation (MDSC). The objective of conducting this assessment is to facilitate the evaluation of the efficacy of these strategies, which is the reason for its implementation. The CDSC and MDSC PLL have been demonstrated to be preferable to other PLLs due to their ability to distinguish between even and odd harmonics. This is due to the fact that each of these harmonics possesses its own distinctive characteristics. This may be attributable to its capacity to independently identify either harmonic. The MATLAB simulation results is provided to demonstrate the exceptional performance of these highly advanced PLLs.

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1. INTRODUCTION

As the need for reliable and environmentally friendly electric power sources continues to climb, the use of power converters has become an increasingly significant component in the development of contemporary power conversion as well as conditioning systems. These systems are designed to ensure that the grid continues to function in a steady manner while also maintaining command over the power factor. Systems such as static VAR compensators, active power restrictions, uninterruptible power supply (UPS), as well as grid-connected photovoltaic or wind power systems are some examples of these types of systems [1,2]. The usage of phase-locked loop (PLL) systems is widespread because they are able to synchronise with the voltage of the grid, which guarantees precise timing and coordination.

Accurate phase tracking of utility voltages is essential for the efficient operation of these systems, and PLL systems are frequently used to achieve this synchronization [3-5]. These systems are very dependent on the precision and durability of the PLL mechanism in order to achieve their desired levels of efficacy and dependability [6]. The approach that is usually employed for grid synchronization procedures is the synchronous reference frames phase-locked loop, which is also often referred to as SRF-PLL.

Extraction of the phase angle and grid voltage frequency, both of which are necessary for synchronizing power converters with the grid, is accomplished by this module [7,8]. When it comes to SRF-PLL, it is necessary for grid voltages to be balanced and devoid of distortion in order to achieve best performance. On the other hand, the insertion of irregular loads and sources of renewable energy into distribution systems leads in the emergence of harmonics, phase angle shifts, and voltage distortions [9-11]. These characteristics have the potential to have a considerable influence on the dynamic performance of SRF-PLLs, particularly when they are operating at high bandwidths.

Two primary methods are used in order to enhance the dynamic performance of SRF-PLL when subjected to distorted circumstances. These methods are the selection of a low-bandwidth option or the incorporation of filters [12,13]. The performance of SRF-PLL is improved by using a low-bandwidth option; however, this option results in a longer reaction time [14]. Alternately, the incorporation of filters into the PLL is a method that assists in achieving precise grid voltage synchronization in spite of the existence of various harmonic grid voltages [15]. Presently available methods for improving SRF-PLL performance via the use of filters may be classified into two distinct groups, pre-filtering and post-filtering, according on the placement of the filter.

There are a few different pre-filtering techniques, two of which being the moving average filters (MAF) as well as the notch filter (NF) respectively [16]. Power converter synchronization with the grid is critical for stable operation, with phase-locked loops (PLLs) commonly used for phase detection. The traditional synchronous rotating frame PLL (SRF-PLL) works well under ideal conditions but struggles with voltage imbalances and harmonics. Advanced PLL structures, such as DDSRF-PLL, DSOGI-PLL, and DSC-PLL, have been developed to address these issues, though they often involve complexity and limited harmonic filtering. Techniques like multiple second-order generalized integrators (MSOGI) and multiple delayed signal cancellation (MDSC) improve harmonic rejection but remain complex for digital implementation. MAF-based PLLs offer simpler harmonic filtering but introduce significant phase delays, with recent enhancements aiming to improve dynamic response and address disturbances under off-normal grid frequencies.

These approaches entail adding a filter behind the input of the PLL in order to smooth out the signal that is being input. It is possible for these filters to increase the efficiency of the phase-locked loop (PLL) in skewed conditions without having an effect on the bandwidth of the PLL [17]. This is accomplished by effectively eliminating high-frequency noise and harmonics. However, in order to guarantee that the phase-locked loop (PLL) continues to operate normally in spite of the existence of the filter, it is necessary to include additional components such as a frequency adaption link and a phase compensation unit. Post-filtering techniques include procedures like phase compensation as well as frequency adaptation [18]. These techniques are used following the time the phase-locked loop (PLL) has retrieved phase as well as frequency information.

This makes it possible to make adjustments and corrections to the PLL output in real time, which guarantees precise synchronization with the grid. The long-term cost and complexity of the system is increased due to the need for complicated control algorithms as well as real-time processing capabilities. Power systems that make use of energy from renewable sources need sophisticated PLL methods, such as pre and post-filtering processes, to enhance their management and integration. Even under challenging grid conditions, these methods ensure that power converters keep operating steadily and efficiently [19-22].

They do this by precisely retrieving fundamental frequency positive sequence (FFPS) components and adjusting for grid distortions. The selection of the PLL approach need to take into account the particular application requirements, the anticipated grid circumstances, and the amount of harmonic filtering that is wanted. This will guarantee the strength and dependability of the performance of power systems. Another option to improve the PLL's performance is to add a filter to the system, such a Second-Order General Integrator (SOGI) module. Two interconnected feedback loops are a part of the SOGI-PLL system. The Park transform receives the anticipated phase angle from one of the loops, while the SOGI module receives the calculated angular frequency from the other loop. The frequency-locked loop (FLL) contains the SOGI module, but the phase-locked loop overlooks it.

As a result of an analogous transformation, the SOGI module performs the functions of a PLL with an in-loop first-order low-pass filter [23]. This effectively reduces the bandwidth of the PLL, which in turn leads to a decrease in dynamic performance. However, despite this decrease in dynamic performance, the SOGI module has basic frequency adaption capabilities, which makes it an important component in PLL systems [24]. Recent research indicates that the Dual Second-Order Generalized Integrator (DSOGI) Phase-Locked Loop (PLL) and its advanced versions are regarded as the most effective method for controlling tough grid

circumstances in three-phase grid-connected inverter systems[25-29]. As a result of its robust architecture and adaptive filtering capabilities, the DSOGI-PLL is able to properly manage large fluctuations, distortions, and phase shifts that may be experienced by these systems. Recent years have seen an increase in the popularity of phase-locked loops (PLLs) based on cascaded delayed signals cancellation (CDSC), multiple delayed signals cancellation (MDSC), and SOGI for their respective advantages [31–35].

The development of SOGI-based PLLs is straightforward, and they are capable of providing efficient harmonic filtering. On the other hand, CDSC-PLLs provide improved harmonic isolation by cascading several delay lines. Further performance enhancement is achieved by MDSC-PLLs by the use of numerous delay lines in parallel, which concurrently target a variety of harmonic frequencies respectively. However, every single form of PLL has its own set of disadvantages. It is possible that SOGI-PLLs will have a worse dynamic performance as a result of the low-pass filter. CDSC-PLLs may be difficult to build and tune, while MDSC-PLLs may need precise modifications to the delay parameters and may be computationally costly. Novel Phase-Locked Loop (PLL) techniques need to be assessed in order to precisely extract fundamental frequency positive sequence (FFPS) components in power systems. This accuracy is critical to the stability and efficiency of grid operations, especially in the presence of harmonics and voltage imbalances. Recent PLL algorithmic improvements have focused on enhancing performance under various grid setups.

The basic PLL is a conventional method for identifying and synchronizing phase angles. It employs a simple feedback loop to align the output signal with a reference. Its primary advantages are its simplicity and ease of implementation. On the other hand, harmonic distortions, voltage swells, sags, and frequency variations cause it to operate badly. To enhance phase detection and harmonic filtering, the DSOGI PLL incorporates two second-order generalized integrators. Phase angle tracking problems arise from the vulnerability of DSOGI PLL to frequency ripple in the presence of significant harmonic distortion [36]. Conversely, to improve phase detection accuracy and harmonic suppression, the CDSC PLL uses delayed signal cancellation techniques. Although this method requires more planning and execution, it doesn't generate frequency ripple and is resistant to harmonic distortion. The MDSC PLL builds on the CDSC approach and improves phase detection and harmonic suppression even further by using multiple delayed signals. It handles complicated waveforms and severe THD situations better, but it requires more computing power and has a more complex design.

Analyses of comparative performance reveal considerable differences between different PLL techniques. While the basic PLL is very error-prone when there is frequency variation, the DSOGI PLL has a respectable level of robustness but still experiences frequency ripple. Precise phase monitoring keeps both CDSC and MDSC PLLs operating at peak efficiency. Under voltage sag conditions, the DSOGI PLL performs somewhat better but still falls short of the traditional PLL, whose performance deteriorates considerably. The MDSC performs better even if the CDSC and MDSC PLLs both maintain stability and accurate phase monitoring. When there are voltage spikes, similar patterns are seen. Recent years have seen an increase in the popularity of phase-locked loops (PLLs) based on cascaded delayed signals cancellation (CDSC), multiple delayed signals cancellation (MDSC), and SOGI for their respective advantages [31–35].

When examined in the presence of harmonics, both in balanced and unbalanced voltage scenarios, the basic PLL performs poorly under considerable harmonic distortion. The DSOGI PLL provides better harmonic filtering but does so at the price of frequency ripple, while the CDSC PLL effectively suppresses harmonics without producing frequency ripple. When it comes to handling situations with considerable THD, the MDSC PLL performs the best. Recent researches demonstrate that complex PLL techniques such as CDSC and MDSC extract accurate FFPS components more accurately than DSOGI PLL and basic PLL under various grid configurations. Despite outperforming the basic PLL, the DSOGI PLL's effectiveness is limited by its susceptibility to frequency ripple in the presence of severe harmonic distortion. However, CDSC and MDSC PLLs perform better across a range of conditions, making them suitable for use in modern power systems that need a high level of precision and reliability[37,38].

In this study, a succinct examination of several phase-locked loops (PLLs) is presented, along with a detailed explanation of the fundamental concepts that underlie each kind. Through the use of MATLAB simulations, it investigates and assesses the efficiency of these sophisticated PLLs across a variety of grid settings. A variety of variations in grid voltage, including fluctuations, distortions, and phase shifts, are simulated and evaluated to see how each PLL responds to these changes[39-41]. The purpose of this research is to advise on the choice and implementation of appropriate PLL approaches for the purpose of improving the efficiency of grid-connected power systems. This will be accomplished by giving a full knowledge of the dynamic responses and resilience of these PLLs in real-world circumstances. Thus the incorporation of filters such as the SOGI module into PLL systems is an efficient method that may be used to enhance grid synchronization and manage voltage distortions.

In spite of the fact that they come with their own unique set of difficulties, advanced PLL approaches, such as DSOGI, CDSC, and MDSC, provide considerable benefits when it comes to the management of demanding grid circumstances. The evaluation of these methods via the use of thorough simulations assists

with comprehending their dynamic effectiveness and resilience, which eventually contributes to the creation of power conversion systems that are more dependable and efficient.

2. ADVANCED PHASE-LOCKED LOOP (PLL)

The incorporation of sources of renewable energy (RESs) as well as non-linear loads has had a substantial impact on power quality over the course of the last ten years, which has resulted in a considerable decline in power systems. Voltage fluctuations, harmonics, and other disturbances are ways in which this degradation presents itself. These disturbances provide significant difficulties to the grid's capacity to maintain its stability and dependability[42]. As a result of the fact that addressing these concerns has become a priority, substantial efforts have been made to improve the rejection of disturbances capacities of SOGI-based synchronous references frame phase-locked loops (SRF-PLLs).

There are several different approaches that have been suggested in order to enhance the disturbance rejection abilities of SRF-PLLs. There are many significant methods that stand out among them, the most notable of which are the Dual Second-Order Generalized Integrator (DSOGI) PLL, the Cascaded Delayed Signal Cancellation (CDSC) PLL, and the Multiple Delayed Signal Cancellation (MDSC) PLL. The purpose of these advanced PLL designs is to improve the capacity of SRF-PLLs to eliminate disturbances like as harmonics as well as voltage fluctuations, which will ultimately lead to an improvement in grid stability as well as power quality respectively. In order to improve noise rejection along with synchronization performance, the DSOGI PLL makes use of a second-order generalized integrator. This is especially beneficial when grid voltage distortions and harmonics are present[40]. By employing this integrator, the DSOGI PLL is able to filter out undesired noise and harmonics in a more efficient manner, hence assuring more precise phase and frequency detection. This is an essential component for the steady integration of RES.

On the other hand, CDSC and MDSC PLLs make use of methods that include delayed signal cancellation in order to accomplish the elimination of harmonics and the improvement of synchronization precision. With the help of these phase-locked loops (PLLs), harmonic components are efficiently suppressed by the selective delaying and summing of the incoming signals. An improvement in the disturbance rejection capacities of the PLLs is achieved via the use of this harmonic cancellation technique. As a result, the PLLs become more resistant to the fluctuations as well as distortions that are brought about by RESs and non-linear loads.

When it comes to minimizing the negative impact that renewable sources as well as non-linear loads have on the stability and quality of the system, the development of sophisticated PLLs that include DSOGI, CDSC, and MDSC marks a major achievement. Improved disturbance rejection capabilities are provided by these phase-locked loops (PLLs), which contribute to the overall durability and dependability of contemporary power grids. These improved PLL designs serve a critical role in sustaining power quality and assuring the steady functioning of power systems in the context of growing integration of renewable energy sources. They do this by enhancing the precision of synchronization and lowering the influence of harmonics as well as voltage fluctuations. The continuous attempts to develop SRF-PLL technologies via the implementation of advanced designs such as DSOGI, CDSC, as well as MDSC have resulted in significant enhancements to the disruptive rejection capacities of these systems. It is crucial that this development be made in order to better manage the issues that are provided by the integration of renewable energy sources and non-linear demands, which will eventually support the stability and dependability of modern power grids.

2.1. SOGI based PLL:

The typical configuration of a frequency-adaptive single-phase SOGI PLL is shown in Figure 1. The transfer functions from the input signal v to its in-phase filtered signal v' and from the input signal v to its filtered quadrature signal v'q are provided in equations (1) and (2), respectively.

$$\left.\begin{aligned} \frac{v'(s)}{v\,(s)} &= \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \\ \left|\frac{v'}{v}\right| &= \frac{k\omega'\omega}{\sqrt{(\omega'^2 - \omega^2)^2 + (\,k\omega'\omega)^2}} \\ \angle\frac{v'}{v} &= \frac{\pi}{2} - \tan^{-1}\left(\frac{k\omega'\omega}{(\omega'^2 - \omega^2)^2}\right) \end{aligned}\right\} \quad (1)$$

$$\left.\begin{aligned} \frac{v'_q(s)}{v\,(s)} &= \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \\ \left|\frac{v'_q}{v}\right| &= \frac{k\omega'^2}{\sqrt{(\omega'^2-\omega^2)^2+(k\omega'\omega)^2}} \\ \angle\frac{v'_q}{v} &= -\tan^{-1}\left(\frac{k\omega'\omega}{(\omega'^2-\omega^2)^2}\right) \end{aligned}\right\} \quad (2)$$

where k is the gain that determines a system's transient response, ω' is the resonant frequency, and ω is the frequency of a signal. Typically, v represents grid voltage in power systems. Equations (1) and (2) make it clear that SOGI-QSG offers low-pass filtering for v' and band-pass filtering for v'q, respectively. Additionally, the following are some additional findings drawn from (1) and (2):

The SOGI-QSG (Second-Order Generalized Integrator - Quadrature Signal Generator) does not satisfy the requirements of the fundamental frequency difference between the input signal and the resonant frequency. This is because the SOGI-QSG seeks to achieve precise gathering of both the quadrature signal and the fundamental frequency signal. It is possible to determine the fundamental frequency of the input signal by using the SRF-PLL, which is represented in the relevant images. This frequency is then provided to the SOGI as the resonance frequency [44]. It is via this way that the SOGI-QSG frequency may be made more adaptable.

Other frequencies are dampened but not completely removed when the resonance frequency signals are sent via the band-pass filtering function of the SOGI-QSG for the v′ component. This feature affects the v′ component. This causes the contaminated grid voltage to have an impure sinusoidal form in v′, with lower-order harmonics predominating. This is the effect of the contamination. When this v′ signal is supplied into the SRF-PLL, it causes mistakes in the calculation of both the phase angle and the frequency. On the other hand, the SOGI-QSG is able to successfully remove the DC component of the input signal in v′, which results in an improvement in the quality of the signal that is extracted.

As a result of its low-pass filtering capabilities, the SOGI-QSG is able to reduce the strength of signals that have frequencies that are greater than its resonant frequency. On the other hand, it allows signals that have frequencies that are up to the resonating frequency to pass through. The contaminated grid voltage has a deformed sinusoidal shape with substantial lower-order harmonics as a consequence of this. The polluted grid voltage is represented by the symbol q. Inconsistencies in phase angle as well as frequency estimations are brought about as a result of the fact that this distorted v'_q is supplied into the SRF-PLL. This occurs as a result of the control action introducing a direct current signal into the grid voltages that are being measured. Irrespective of the gain k and the frequency of the resonant, the q component can never be more than 90 degrees behind the v component. This is the case regardless of the q component.

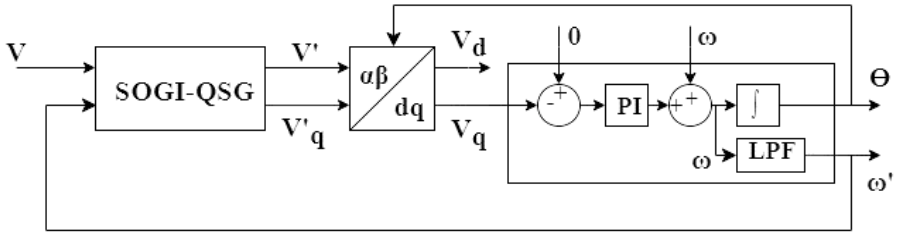


Figure 1. The general structure of frequency adaptive single phase SOGI PLL

In order to guarantee the precise retrieval of the basic frequency and to lessen the influence of harmonics, the filtering activity of the SOGI-QSG is of the utmost importance. The existence of considerably lower-order harmonics and the introduction of DC components, on the other hand, provide obstacles for the purpose of maintaining exact estimations of phase angle and frequency. The efficiency of the SRF-PLL may be negatively impacted as a result of these errors, especially when the grid conditions are skewed. The SOGI-QSG is capable of providing essential filtering capabilities and enhances the quality of the extracted signals by removing DC components. However, in order to improve the overall performance and accuracy of the SRF-PLL in practical applications, it is necessary to address the inherent challenges that are associated with lower-order harmonics and phase lag.

In a three-phase system, a separate SOGI-QSG is used for each phase to extract the fundamental signal and its orthogonal component. These extracted signals are then used to calculate the FFPS components according to ISC theory, as detailed in equation (3-5), and subsequently input into the SRF-PLL, as shown in Fig. 2.

$$v_{\mathrm{a}}'^{+} = \frac{1}{3}\left[\left\{v_{\mathrm{a}}' - \frac{1}{2}(v_b' + v_{\mathrm{c}}')\right\} - \frac{\sqrt{3}}{2}\left\{v_{b\mathrm{q}}' - v_{c\mathrm{q}}'\right\}\right] \quad (3)$$

$$v_{\mathrm{b}}'^{+} = v_{\mathrm{a}}'^{+} - v_{\mathrm{c}}'^{+} \quad (4)$$

$$v_{\mathrm{c}}'^{+} = \frac{1}{3}\left[\left\{v_{\mathrm{c}}' - \frac{1}{2}(v_a' + v_{\mathrm{b}}')\right\} - \frac{\sqrt{3}}{2}\left\{v_{a\mathrm{q}}' - v_{c\mathrm{q}}'\right\}\right] \quad (5)$$

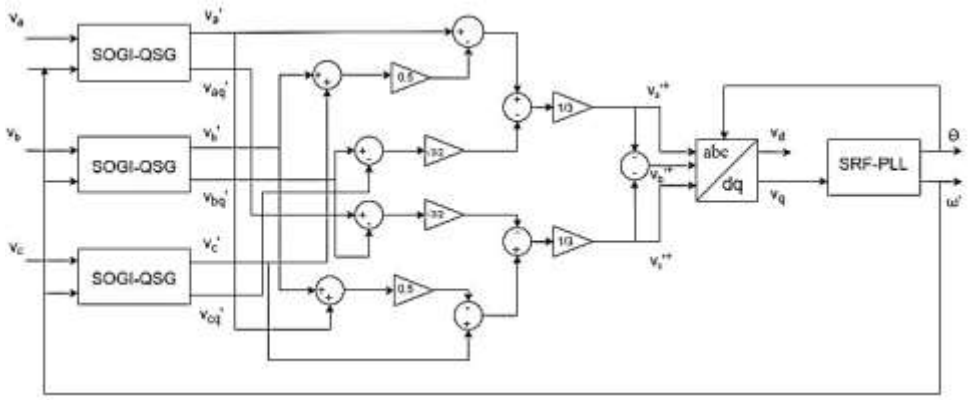


Figure 2. The general structure of frequency adaptive three phase SOGI PLL

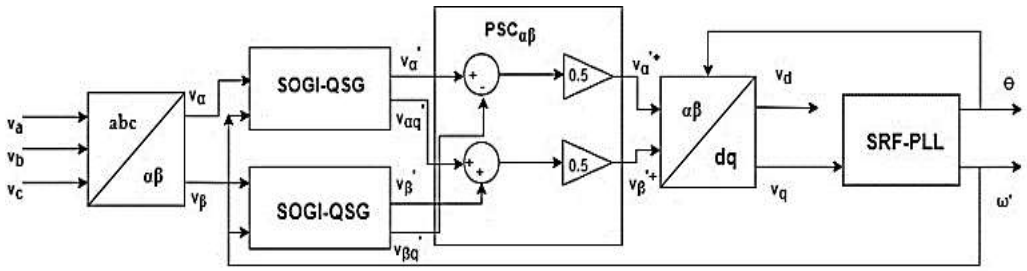


Figure 3. The general structure of frequency adaptive DSOGI PLL

The PLL design is greatly simplified when system signals are analyzed in the αβ reference frame. This is because the need for three SOGI-QSGs (Second-Order Generalized Integrator - Quadrature Signal Generators) is reduced to only two. As a result of this simplification, a DSOGI-based PLL is developed. This PLL is represented in pertinent images, such as Figure 3. This method is similar to the dual enhanced phase-locked loop (DEPLL) technique, in which the θ β component of the input signal acts as the quadrature to the α α component [45]. This strategy, on the other hand, is not useful for unbalanced systems because it does not fully resolve the disparities that are brought about by unbalanced situations. Because it is entirely focused on getting precise frequency information from the PLL, the DSOGI-based PLL is able to circumvent this constraint. By using this technique, the performance of the PLL is improved across a wide range of grid situations, including ones that include substantial imbalances. The DSOGI-PLL is able to deliver more robust and dependable synchronization since it focuses on frequency extraction. This is true regardless of whether the input signals are distorted or unbalanced.

Furthermore, the calculation of the positive sequence components in the αβ reference frame is accomplished by using the Instantaneous Symmetrical Components (ISC) theory. This theory has been extensively studied and is represented by particular equations, such as equation (4) in reference [5]. When it comes to precisely estimating the positive sequence components, which are necessary for good grid synchronization and the maintenance of the stability of power systems, ISC theory is absolutely critical. With the use of this theory, it is possible to distinguish between the positive sequence components and the negative sequence components and the zero sequence components, which ultimately results in an improvement in the PLL's overall accuracy and performance.

It is possible for the DSOGI-based PLL to efficiently address the obstacles that are provided by imbalanced and distorted grid settings. This is accomplished by using the $\alpha\beta$ αβ reference frame and the ISC theory techniques. This leads to improvements in frequency tracking and phase synchronization, both of which are essential for the incorporation of renewable energy sources and the stability of current power grids. Because of its capacity to correctly extract and make use of frequency information, the DSOGI-PLL is able to keep its synchronization and stability intact, even when there are considerable grid disturbances present.

The DSOGI-based PLL is a major improvement in the design of PLLs because it simplifies the requirements for the system and improves performance in grid settings that are difficult to manage. This technique offers a resilient solution for contemporary power systems by concentrating on frequency extraction and making use of ISC theory for the computation of positive sequence components. This approach guarantees dependable synchronization and enhances grid stability.

$$v_{\alpha}'^{+} = \frac{1}{2}\left(v_{\alpha}'^{+} - v_{\beta q}'^{+}\right) \tag{6}$$

$$v_{\beta}'^{+} = \frac{1}{2}\left(v_{\alpha q}'^{+} + v_{\beta}'^{+}\right) \tag{7}$$

2.2. CDSC based PLL:

The monitoring of the positive-sequence fundamental voltage component is the primary focus of a grid-synchronization phase-locked loop (PLL) in the event that the grid voltage is subject to distortion. The dq-frame, which is a revolving reference frame that is synchronized with the grid, indicates the presence of this component in the form of a direct current (DC) signal. When harmonics are present, the harmonics that were previously present in the ABC and αβ-frames convert into harmonics in the dq-frame. This transformation occurs when harmonics are present. The half-wave symmetry that these harmonics possess in sinusoidal waveforms causes them to be moved by one order in the dq-frame from the original waveform.

Additionally, the harmonics that are present in the dq-frame have the potential to negatively impact the PLL's capability to reliably monitor the fundamental frequency. On the other hand, since these harmonics have a feature known as half-wave symmetry, it is possible to efficiently eradicate them by using a method that is known as delayed signal cancellation (DSC). As part of the DSC process, the signal is added to a delayed version of itself while it is being processed. When this delay is introduced and the signals are added together, the harmonics, which have opposing phases at particular times, cancel each other out without causing any interference. When this cancellation occurs, the basic voltage component is not impacted in any way.

Harmonic removal may be accomplished by the use of the delayed signal cancellation approach, which makes use of the symmetrical features of sinusoidal harmonics. The phase-locked loop (PLL) is able to maintain exact synchronization with the fundamental frequency of the grid voltage, despite the existence of distortions, since it ensures that the harmonics are canceled out. This capacity is essential for preserving the stability of the grid and assuring the dependable functioning of systems that are linked to the grid, particularly in situations when voltage distortion is produced by nonlinear loads or other disturbances.

Essentially, the DSC approach improves the resilience of the PLL by filtering out harmonic distortions while maintaining the integrity of the fundamental frequency component. This is accomplished by conserving the fundamental frequency component. This enables the phase-locked loop (PLL) to maintain its exact synchronization with the grid, which guarantees that the system will continue to function in an efficient and dependable manner even when there are voltage disturbances in the grid.

In general, the suggested DSC operator can be expressed as follows for any random dq-frame voltage signal v(t) as

$$\mathrm{DSC_n} = \frac{1}{2}\left[v_h(t) + v_h\left(t - \frac{T}{n}\right)\right] \tag{8}$$

Where, n-delay factor and T-grid fundamental period. It is possible to produce an out-of-phase signal by varying the delay times (T/n). The time interval from t = 0 to the point that the signal crosses zero negatively is the minimum delay needed by the DSC operator. For instance, the following delay durations are conceivable to eliminate a 4th-order harmonic frequency signal: T/8, (T/8 + T/4), (T/8 + 2T/4), and (T/8 + 3T/4). Generally, the possible delay times T/n to eliminate the hth harmonic frequency signal are

$$\frac{T}{n} = \frac{T}{2h} + k\frac{T}{h} \qquad \forall\, k < h - 0.5 \;\&\; k \epsilon N_0. \tag{9}$$

The harmonics of the types 2k+1, 4k+2, 8k+4, 16k+8, and 32k+16 are eliminated by the DSC operators DSC2, DSC4, DSC8, DSC16, and DSC32, respectively. These operators are intended to remove

harmonics. In order to remove many harmonics, it is common practice to utilize several operators in conjunction with one another. This is due to the fact that each operator targets a distinct harmonic order. Harmonics of the shapes 2k, 4k, 8k, 16k, and 32k are able to flow through without being attenuated by these DSC operators. The operators are cascaded, which successfully eliminates all lower-order harmonics, which is done to guarantee that thorough harmonic removal is achieved. Based on the information provided in references [15–18], this cascading results in the formation of the cascaded delayed signal cancellation (CDSC 2, 4, 8, 16, 32) operator. This operator was developed with the express purpose of serving applications that fall under the dq reference frame. However, if it is used in the ABC frame, it will remove the fundamental frequency component, which is necessary for grid synchronization when using SRF-PLL. This is because the fundamental frequency component.

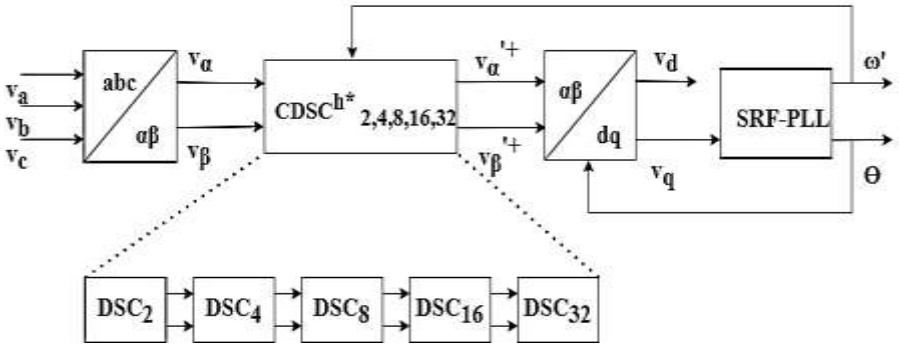


Figure 4. The general structure of frequency adaptive CDSC PLL

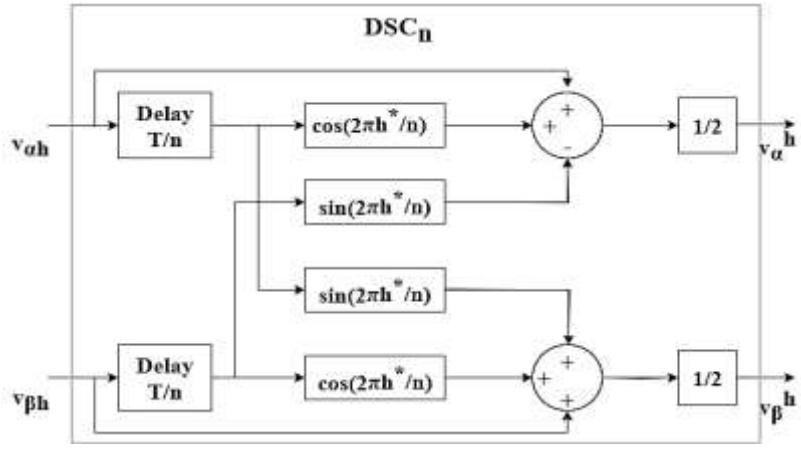


Figure 5. Time domain implementation of DSCn operator

In order to ease the analysis of alternating current (AC) systems, the dq reference frames are used to undergo the transformation of three-phase signals into a two-axis system. These reference frames are capable of rotating at any frequency and in any direction; nevertheless, they are commonly aligned with the fundamental frequency and the direction in which the rotation of the resulting vector occurs. As a consequence of this, the basic frequency components that are balanced in the ABC frame are transformed into DC quantities in the dq frame, which therefore makes them simpler to control. There are numerous harmonics that may be handled by the Composite Delayed Signal Cancellation (CDSC) operator, which includes CDSC2,4,8,16,32. This operator is especially intended to enable signals of the 32k harmonic order in the dq frame, which converts to 32k ± 1 harmonics in the ABC frame. Through the use of this feature, the fundamental frequency component is efficiently isolated. On the other hand, the CDSC2,4,8,16,32 operator results in a total delay time of 31 degrees and 32 seconds.

In order to cut this delay down to 15T/16, a simpler version of the CDSC2,4,8,16 is used. However, this comes at the expense of not being able to get rid of all 16K harmonics in the dq frame. Because of this constraint, it is necessary to use a SRF-PLL with a reduced bandwidth in order to accomplish grid synchronization that is successful. In spite of this, the CDSC operator imposes a temporal delay inside the SRF-PLL control loop, which has the potential to negatively impact the dynamic performance of the system. The

transfer of the equivalent CDSC operator from the dq frame to the αβ frame, as stated by equation 6, is of utmost importance for achieving greater stability. This transfer ensures that the system continues to be stable and efficient while performing grid synchronization activities during grid synchronization.

$$\begin{bmatrix} DSCn[v_{\alpha h}] \\ DSCn[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} cosh^{*}\theta & -sinh^{*}\theta \\ sinh^{*}\theta & cosh^{*}\theta \end{bmatrix} * \begin{bmatrix} DSCn[v_{dh}] \\ DSCn[v_{qh}] \end{bmatrix} \quad (10)$$

Where,

$$DSC_n[v_{dqh}] = \frac{1}{2}\left[v_{dq}h(\omega t) + v_{dq}h(\omega t - T/n)\right] \quad (11)$$

In the equation shown above, the symbol ω represents the standard angular frequency, h represents the harmonic order, and h*= ±h indicates the particular positive sequential harmonic frequency component that is to be recovered by the CDSC operator. When it comes to positive sequence signals, the "+" sign is used, whereas the "−" sign is employed for negative sequence signals, with the equation Θ=ωt employed. Equation (12) provides the condensed version of equation (10) in its simple form.

$$\begin{bmatrix} DSC_n[v_{\alpha h}] \\ DSC_n[v_{\beta h}] \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_{\alpha h}(\omega t) + v_{\alpha h}\left(\omega t - \frac{T}{n}\right)cos\frac{2\pi h^{*}}{n} - v_{\beta h}\left(\omega t - \frac{T}{n}\right)sin\frac{2\pi h^{*}}{n} \\ v_{\beta h}(\omega t) + v_{\beta h}\left(\omega t - \frac{T}{n}\right)cos\frac{2\pi h^{*}}{n} + v_{\alpha h}\left(\omega t - \frac{T}{n}\right)sin\frac{2\pi h^{*}}{n} \end{bmatrix} \quad (12)$$

When dealing with simple digital controller duties like transit delay, multiplication, and summation, the CDSC operator usually performs well. This issue can be mitigated by having a multiple of 32 for the total number of samples inside a fundamental time period T. As shown in figure 4, T needs to be updated regularly using SRF-PLL because it fluctuates in many applications. And, Figure 5 shows the DSCn operator time domain implementation.

2.3. MDSC based PLL:

To address the challenges associated with total delay time and storage in digital control systems, a modified version of the delayed signal cancellation (DSC) operator, known as the multiple delayed signal cancellation (MDSC), is proposed. This innovation aims to enhance efficiency while reducing computational complexity. MDSC, an advancement over CDSC, operates by employing multiple delays of varying durations on a test signal until the combined sum of the signal and its delayed versions approaches zero. This iterative process aims to enhance signal clarity by effectively cancelling out unwanted components like noise or interference[46]. MDSC builds upon CDSC's principles of phase manipulation and delay adjustment within digital control systems, ensuring improved signal fidelity through iterative refinement of delay parameters until desired signal enhancement or cancellation is achieved.

In the MDSC approach, the delay times are strategically chosen as integer multiples of T/15 , where T represents the fundamental time period. This design ensures that the delay times do not exceed the fundamental period T itself. Consequently, this variant is named MDSC15. The maximum delay time of MDSC15 is consistently 14T/15, which is notably shorter than the delay time associated with CDSC variants.

When implemented in the dq frame, MDSC15 effectively eliminates all harmonic frequency signals apart from those corresponding to 15k frequency signals. This implies that MDSC15 selectively passes only 15k±1 frequency signals from the abc frame. It's noteworthy that MDSC15 behaves differently from CDSC in terms of the harmonics it passes. Specifically, MDSC15 permits even harmonics such as 14 and 16, unlike CDSC, which primarily passes odd harmonics like 15 and 17. The general structure of frequency adaptive MDSC PLL is shown in figure 6.

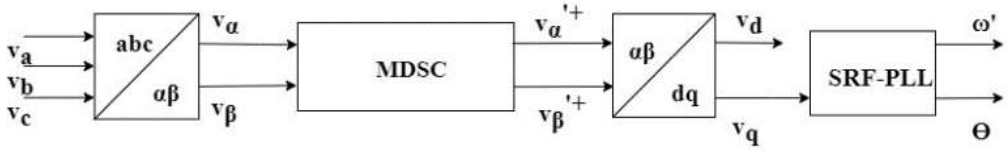


Figure 6. The general structure of frequency adaptive MDSC PLL

In practical applications, MDSC15 offers certain advantages over CDSC. Due to the absence of even harmonics in typical power system scenarios, SRF-PLL bandwidth can be set higher for MDSC15 compared to CDSC, thereby potentially improving system performance. However, this choice should be made considering the specific requirements and characteristics of the application [19].To integrate MDSC15 into the control loop

effectively, its dq equivalent is transformed onto the αβ frame using a specific mathematical equation 13, ensuring seamless compatibility and operation within the desired framework.

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} cosh^{*}\theta & -sinh^{*}\theta \\ sinh^{*}\theta & cosh^{*}\theta \end{bmatrix} * \begin{bmatrix} MDSC_{15}[v_{dh}] \\ MDSC_{15}[v_{qh}] \end{bmatrix} \quad (13)$$

Where, $MDSC_{15}[v_{dqh}] = \frac{1}{15}\sum_{l=0}^{14}[v_{dq}h(\omega t - Tl/15)]$

The simplified form of equation (13) is provided in equation (14).

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \frac{1}{15}\begin{bmatrix} v_{\alpha h}(\omega t)+\sum_{l=0}^{14}\{v_{\alpha h}\left(\omega t-\frac{Tl}{15}\right)cos\frac{2\pi h^{*}l^{*}}{15} - v_{\beta h}\left(\omega t-\frac{Tl}{15}\right)sin\frac{2\pi h^{*}l^{*}}{15}\} \\ v_{\beta h}(\omega t)+\sum_{l=0}^{14}\{v_{\beta h}\left(\omega t-\frac{Tl}{15}\right)cos\frac{2\pi h^{*}l^{*}}{15} + v_{\alpha h}\left(\omega t-\frac{Tl}{15}\right)sin\frac{2\pi h^{*}l}{15}\} \end{bmatrix} \quad (14)$$

3. DESIGN AND PERFORMANCE EVALUATION OF AN ADVANCED PLL

The DSOGI, CDSC, and MDSC based Phase-Locked Loop (PLL) are each shown in Figure 7: Figure 7a, Figure 7b, and Figure 7c, respectively. The advanced PLL block receives its input from a programmable source, which enables the block to be tested under different grid situations with more flexibility. In addition, the appendix has a full explanation of the MATLAB functions that must be used for Phases a, b, and c in order to accommodate a different grid condition. These operations are necessary for simulating and assessing the efficiency of the PLLs under different circumstances. This helps to ensure that the PLLs operate in a reliable and accurate manner across a variety of electrical grid conditions.

The sophisticated PLLs were subjected to exhaustive testing with the help of MATLAB simulations in order to investigate their behavior under a variety of grid settings. The main factor that determines the accuracy of these contemporary phase-locked loops (PLLs) is the caliber of the frequency ω in the SRF-PLL. Therefore, it is of the utmost importance to guarantee a precise frequency in the SRF-PLL, since this has a direct influence on the reliability and efficacy of the DSOGI, CDSC, and MDSC-based PLL systems. The simulations are helpful to comprehend how each PLL reacts to changes as well as disturbances in the grid, which provides vital insights on the resilience and efficiency of the PLLs.

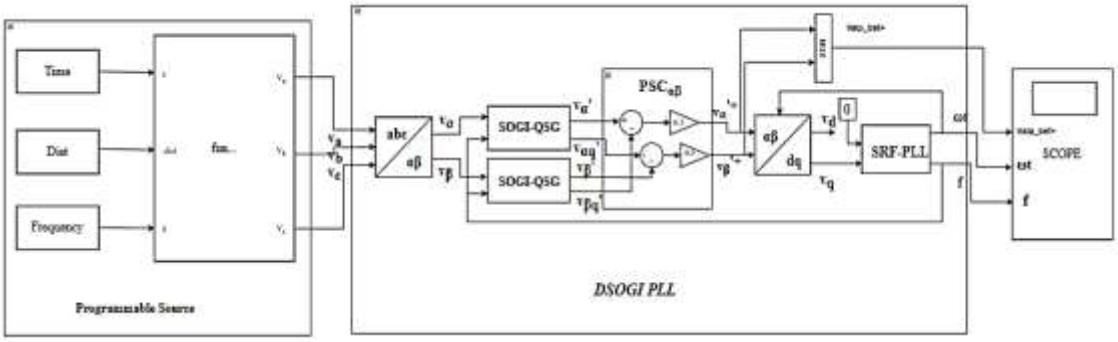


Figure 7a. Design and modelling of DSOGI PLL

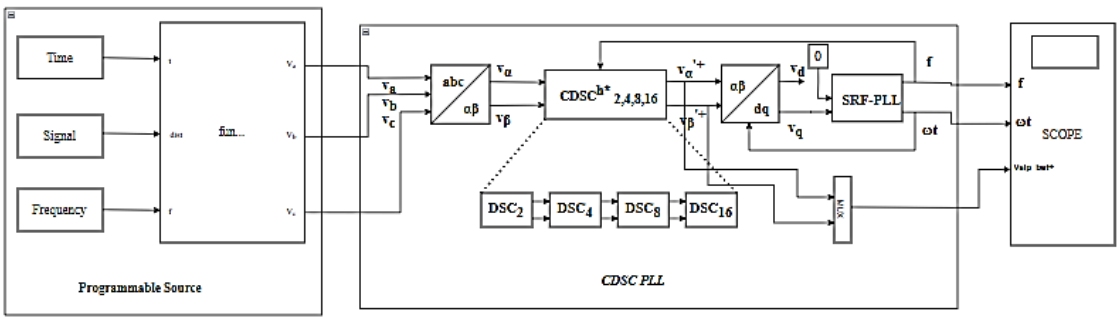


Figure 7b. Design and modelling of CDSC PLL

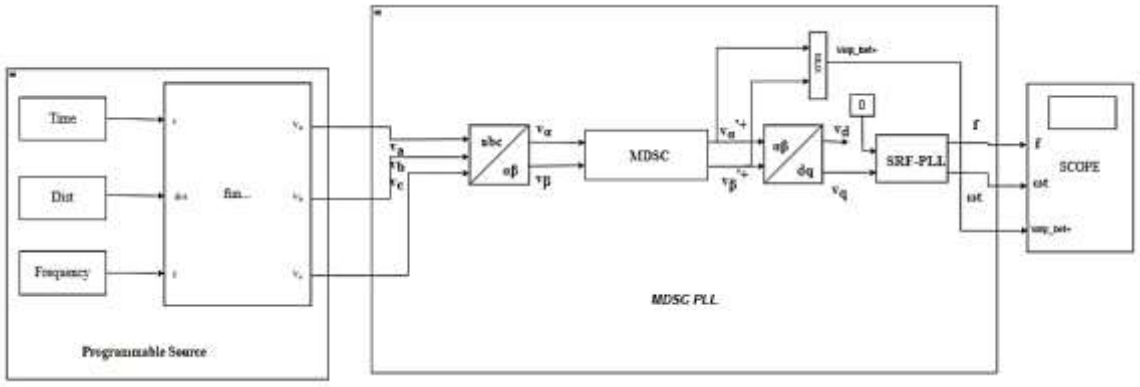


Figure 7c. Design and Modelling of MDSC PLL

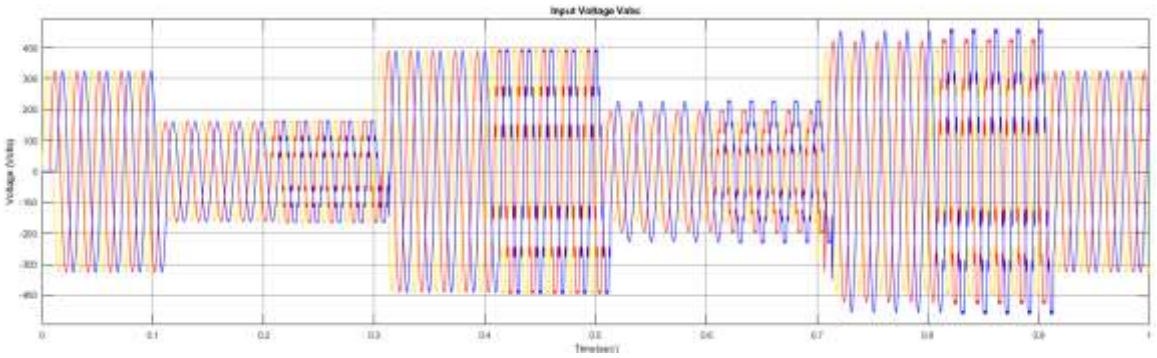
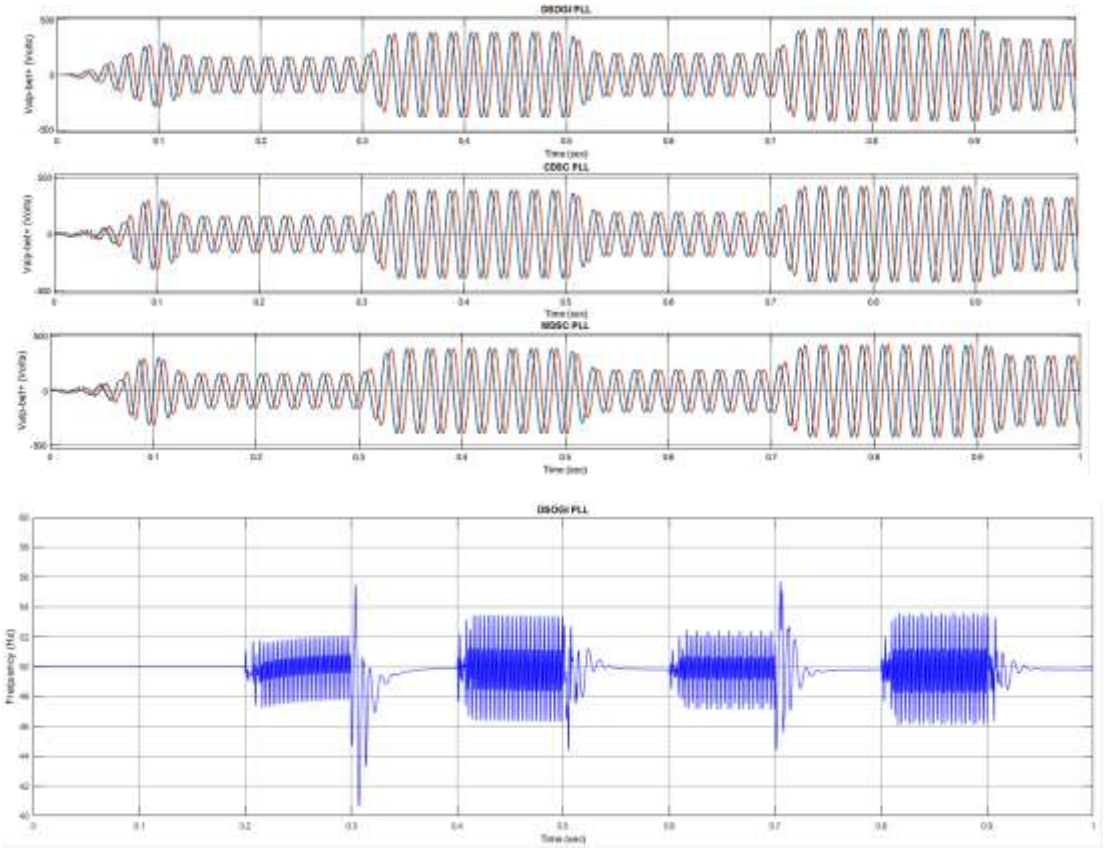


Figure 8a. Input voltage Vabc



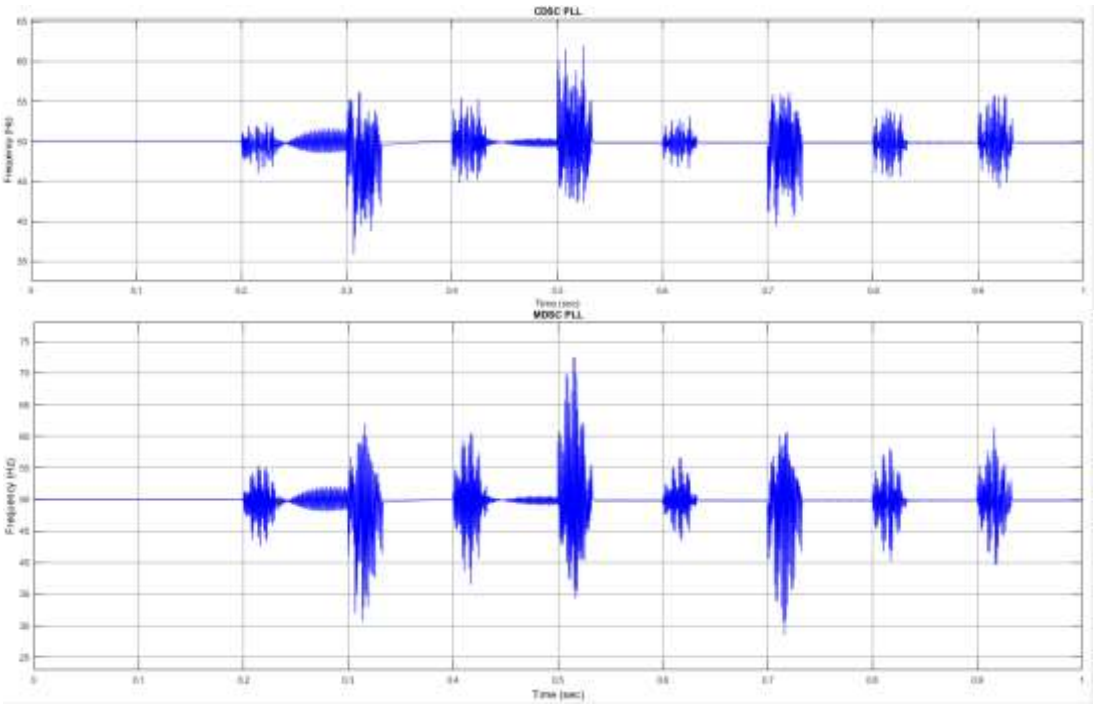


Figure 8b. Simulation results of advanced PLL outputs (Voltage & Frequency) for various grid conditions.

i. Frequency Variation:

An abrupt increase in the grid frequency from its nominal value of 50 Hz to 48 Hz occurs at the time t=0.3 seconds. The frequency variation is shown in Figure 8b. In the process of studying the performance of Phase-Locked Loops (PLLs) under this frequency setting, it has been noted that all PLLs have a strong steady-state tracking capability, even when considerable frequency jumps are present. The fact that they are able to maintain synchronization and properly monitor the grid frequency despite rapid and significant fluctuations is shown by this. When compared to the PLLs that are based on Composite Delayed Signal Cancellation (CDSC) and Multiple Delayed Signal Cancellation (MDSC), the DSOGI-PLL stands out due to its higher tracking speed. This enables it to adjust to changes in frequency more rapidly than the other PLLs that were tested.

On the other hand, when the long-term tracking performance is taken into consideration, all PLLs exhibit comparable tracking speeds and degree of precision[47,48]. In spite of the fact that the DSOGI-PLL provides an early advantage in terms of tracking speed, the CDSC and MDSC-based PLLs eventually catch up and maintain synchronization with the same level of accuracy. The PLLs have a very little amount of variation in their frequency tracking, which suggests that even while their initial reactions could be somewhat different from one another, their overall capability to precisely follow the grid frequency is not affected by this variation. All of the phase-locked loops (PLLs) that were put through their paces had robust steady-state tracking capabilities despite considerable frequency fluctuations. However, the DSOGI-PLL demonstrated a more rapid response to changes in frequency. Over the course of time, the CDSC and MDSC-based PLLs achieve the same level of speed and accuracy as the DSOGI-PLL. This guarantees a dependable performance in terms of preserving grid synchronization despite the presence of several frequency circumstances.

ii. Balanced voltage with Sag

The fundamental balanced voltage sag, which is seen in Figure 8b, takes place during the span of time ranging from t = 0.1 seconds to t = 0.2 seconds over the course of the time period. Over the course of this time period, all three Phase-Locked Loops (PLLs)—DSOGI-PLL, CDSC-based PLL, and MDSC-based PLL—exhibit adequate performance in maintaining phase angle tracking. Because of the balanced nature of the voltage sag, it guarantees that the main voltage levels will decline in a consistent manner throughout all phases, without producing any distortions or asymmetries. This consistent decline contributes to the maintenance of stable circumstances when phase angle monitoring is performed.

Under these circumstances, the lack of frequency ripple during the voltage sag is the primary component that contributes to the PLLs' ability to work well. In this balanced situation, there is no presence of frequency ripple, which is a significant factor that may lead to oscillations and instability in phase angle

tracking. As a consequence of this, the phase-locked loops (PLLs) are able to continue to precisely monitor the phase angle of the main voltage without being influenced by potential disturbances that would otherwise make the tracking process more complicated. The DSOGI-PLL, CDSC-based PLL, and MDSC-based PLL exhibit commendable phase angle tracking performance during the balanced voltage decline from t = 0.1 seconds to t = 0.2 seconds. In this balanced sag situation, the absence of frequency ripple guarantees that all three phase-locked loops (PLLs) are able to keep their phase angle tracking precise and steady. This effectively demonstrates the resilience and dependability of the PLLs under such grid settings.

iii. Balanced harmonics voltage with sag

As shown in Figure 8b, the fundamental balanced voltage sag with harmonics is shown across the time range from t=0.2 seconds to t=0.3 seconds. It is at this time that more harmonics, notably the fifth, seventh, eleventh, and thirteenth, are added, which ultimately leads to a large total harmonic distortion (THD) of roughly 27 percent. Due to the fact that the superposition of these higher-order harmonics generates a more distorted and demanding environment for phase angle tracking by Phase-Locked Loops (PLLs), the existence of these harmonics makes the voltage sag situation more complicated. It has been found that the DSOGI-PLL, which is one of the PLLs that were assessed, displays frequency ripple as a reaction to the harmonic distortion effect. Because of this frequency ripple, tracking errors in the phase angle are introduced, which makes it more difficult for the DSOGI-PLL to precisely follow the real phase of the basic voltage component. Because of the existence of harmonics, the generally steady functioning of the DSOGI-PLL is disrupted, which results in considerable mistakes in phase angle tracking being produced.

On the other hand, the CDSC and MDSC-based PLLs exhibit higher performance when the same harmonics are found in the environment. These phase-locked loops (PLLs) are developed using sophisticated filtering and delay operator methods, which enables them to regulate and minimize the influence of harmonic distortions in a more effective manner. PLLs that are based on CDSC and MDSC are able to maintain precise phase angle tracking despite the substantial total harmonic distortion (THD). This allows them to avoid the frequency ripple and tracking mistakes that are a problem for the DSOGI-PLL.

Therefore, it is possible to draw the conclusion that CDSC and MDSC-based PLLs perform more successfully than DSOGI-PLL in situations that include significant harmonic distortion, such as the one represented from t=0.2 seconds to t=0.3 seconds with a total harmonic distortion (THD) of around 27 percent. Because of their sophisticated design, they are able to deal with the difficulties that are brought about by harmonics. This enables them to provide phase angle tracking that is more dependable and precise, and it also highlights their resilience in terms of sustaining performance under tough grid settings.

iv. Balanced voltage with Swell

An important balanced voltage swell takes place throughout the time period from t=0.3 seconds to t=0.4 seconds, as shown in Figure 8b. This swell is responsible for the necessary balanced voltage. An example of a balanced swell scenario is created when the principal voltage levels grow in a manner that is consistent across all phases throughout this time. The fact that this uniform increase in voltage does not generate any asymmetries or distortions makes it a condition that is generally stable for phase angle tracking via Phase-Locked Loops (PLLs). It has been determined that the phase angle tracking performance of the DSOGI-PLL, CDSC-based PLL, and MDSC-based PLL during this balanced voltage swell is adequate. The lack of frequency ripple during the tracking process is the most important aspect that contributes to their excellent performance. This balanced voltage swell does not exhibit any phase angle tracking changes or instability due to the absence of frequency ripple, which is a potential source of instability. That the phase-locked loops (PLLs) are able to continue to precisely monitor the phase angle of the basic voltage component without being impacted by potential disturbances is ensured by the lack of this component.

As a consequence of this, all three phase-locked loops (PLLs)—DSOGI-PLL, CDSC-based PLL, and MDSC-based PLL exhibit a strong performance in terms of phase angle tracking during the balanced voltage swell that occurs from t=0.3 seconds to t=0.4 seconds. The fact that they are able to keep their phase angle tracking precise and steady under these circumstances is evidence of their efficiency and dependability in dealing with balanced voltage swells. This helps to ensure that grid operations continue to be synchronized and stable.

v. Balanced harmonics voltage with swell

When conducting an examination of voltage swells with harmonics, it is of the utmost importance to have a well-rounded understanding of the behavior of various systems in reaction to these disturbances. In this particular scenario, a fundamental balanced voltage swell takes place between the time periods of 0.4 seconds and 0.5 seconds, as seen in Figure 8b. Additional harmonics, notably the fifth, seventh, eleventh, and thirteenth. These harmonics are injected into the system during this swell. The incorporation of these harmonics is

intended to generate a total harmonic distortion (THD) of around 27 percent, which has a major impact on the quality of the waveform as a whole.

The Dual Second Order Generalized Integrator (DSOGI) system is remarkable for demonstrating frequency ripple when compared to other systems that are being evaluated for their performance under similar circumstances. Due to the fact that it causes tracking errors in the phase angle, this frequency ripple is a major concern. These mistakes may have a negative impact on the system's ability to maintain proper voltage regulation and power quality. On the other hand, it has been shown that systems such as CDSC (Conventional DSC) and MDSC (Modified DSC) work more successfully when harmonics are present. The ability of CDSC and MDSC to manage these harmonics without generating large frequency ripple is the primary benefit that sets them apart from DSOGI. This capacity effectively reduces the amount of phase angle tracking mistakes that occur. The significance of choosing proper technologies for regulating voltage swells and harmonics in power networks is highlighted by this improved performance. This is especially true in situations where it is necessary to maintain a high level of power quality. When compared to DSOGI, CDSC and MDSC are more successful in managing harmonics, which implies that they are more suited for situations that have high harmonic distortion. Additionally, they provide performance that is more stable and dependable that is more consistent.

vi. Unbalanced voltage with Sag

Figure 8b depicts an imbalance in the fundamental voltage that takes place between the time intervals of 0.5 second and 0.6 seconds. There are three separate per-unit voltage levels that are experienced by each phase of the system throughout this time period: phase A has a voltage of 0.5 per unit, phase B has a voltage of 1 per unit, and phase C has a voltage of 0.7, respectively. When it comes to maintaining the stability of the system and the quality of the electricity, this mismatch may cause considerable issues. The fact that there is no frequency ripple during this voltage imbalance is one of the most important findings that can be made from Figure 8b. The absence of frequency ripple is an essential component since it has a direct impact on the functioning of phase-locked loops (PLLs), which are used for the purpose of synchronizing the phase angle of the voltage with a reference signal. All three modern phase-locked loops (PLLs) are able to maintain their superior phase angle tracking even when they are subjected to fundamental imbalance since there is no frequency ripple. A high degree of performance is needed for the dependable functioning of power systems. This is because precise phase angle tracking is necessary for a variety of activities, including grid synchronization, power factor correction, and efficient power distribution.

The findings that are displayed in Figure 8b reveal that modern PLLs are well-prepared to manage fundamental imbalances without compromising their phase angle tracking capabilities. This is demonstrated by the fact that they are adequately equipped. The efficiency of current PLL designs in preserving system stability and assuring continuous, dependable operation in a variety of power network circumstances is highlighted by the fact that they are able to withstand voltage imbalance without causing frequency ripple.

vii. Unbalanced harmonics voltage with sag

In this particular circumstance, the fundamental voltage imbalance continues to be consistent with the findings made in the past. Additionally, harmonics of the fifth, seventh, eleventh, and thirteenth orders are injected, resulting in a total harmonic distortion (THD) of roughly 27 percent. Figure 8b includes a representation of this phenomenon for the period of time ranging from $t = 0.6$ seconds to $t = 0.7$ seconds. Due to the existence of these harmonics, the voltage waveform is further complicated, which presents a problem for the stability of the system as well as the quality of the power. DSOGI, which stands for Dual Second Order Generalized Integrator, is one of the systems that stands out for its ability to show frequency ripple on many systems. It is important to note that this frequency ripple is crucial because it causes tracking errors in the phase angle, which may result in a decrease in the system's performance in terms of both accuracy and dependability. The frequency ripple that was seen in DSOGI is evidence that it has difficulty maintaining exact phase angle tracking when there is a significant amount of harmonic distortion present.

CDSC, which stands for conventional DSC, and MDSC, which stands for modified DSC, both exhibit greater performance when subjected to these circumstances. In spite of the existence of harmonics, these systems are able to keep their phase angle tracking precise because they do not display frequency ripple. The robustness and dependability of CDSC and MDSC are highlighted by the fact that they are able to effectively manage harmonic distortion without creating tracking mistakes. Because of this, they are better suited for settings in which it is very important to keep the power quality at a high level, particularly when there is a substantial amount of harmonic distortion present.

The comparison demonstrates that while DSOGI may be beneficial in situations where there is a low amount of harmonic content, it is less successful in settings where there is a significant total harmonic distortion (THD). CDSC and MDSC, on the other hand, are both better capable of handling complicated waveforms,

which allows them to guarantee consistent and dependable performance even when faced with difficult circumstances. This demonstrates how important it is to pick suitable solutions depending on the unique needs of the power network, especially in situations where there is a substantial amount of harmonic distortion.

viii. Unbalanced voltage with Swell

The basic voltage variations that occur between the periods t = 0.7 seconds and t = 0.8 seconds are shown in Figure 8b. Over the course of this time period, the voltages that are measured per unit for phases A, B, and C are 0.5, 1, and 0.7, respectively. It is clear from these data that there is a considerable imbalance in the voltage levels that are present throughout all three phases. In spite of this imbalance, one of the most important observations that can be made from Figure 8b is that there is no frequency ripple, which is essential for ensuring that the system remains stable.

The performance of phase-locked loops (PLLs) is significantly impacted by the lack of frequency ripple, which plays a vital role. In order to ensure that power systems are operating accurately and consistently, phase-locked loops (PLLs) are absolutely necessary for synchronizing the phase angle of the voltage with a reference signal. There is a possibility that phase angle tracking mistakes will occur when there is frequency ripple present. This may result in inefficiencies and instability. On the other hand, phase-locked loops (PLLs) are able to keep their phase angle tracking exact even when there is fundamental imbalance since they do not have frequency ripple.

In this particular circumstance, the data that is given in Figure 8b reveals that all three modern PLLs display good phase angle tracking. The fact that this is the case demonstrates that contemporary PLL architectures are resilient and able to deal with voltage imbalances without impairing their performance. Having the capability to correctly measure the phase angle assures that different components of the power system, such as inverters, grid synchronizers, and power factor correction devices, will operate in a dependable manner. Taking everything into consideration, the image that can be seen in Figure 8b demonstrates how successful modern PLLs are in regulating basic voltage imbalances. These systems are able to maintain high levels of precision and stability, which is necessary for the effective functioning of power networks, since there is no phenomenon known as frequency ripple. Because of its resilience against voltage imbalance, improved PLL designs are becoming more important in current applications of electrical engineering. These designs provide a dependable solution for preserving power quality and system stability.

ix. Unbalanced harmonics voltage with swell

In this particular scenario, the proportion of basic voltage imbalance is considered to be the same as it was in the previous experience. In addition, the fifth, seventh, eleventh, and thirteenth harmonics are added to the final result in order to achieve a total harmonic distortion (THD) of around 27 percent. In this scenario, the basic voltage imbalance remains consistent with previous conditions. Additionally, harmonics of the fifth, seventh, eleventh, and thirteenth orders are introduced, resulting in a total harmonic distortion (THD) of approximately 27 percent. This is illustrated in Figure 8b during the time interval from t = 0.8 seconds to t = 0.9 seconds. The inclusion of these harmonics significantly complicates the voltage waveform, posing a challenge for maintaining power quality and system stability.

Table 1. Performance of advanced PLL under various grid conditions.

Grid Conditions / PLL	DSOGI	CDSC	MDSC
Frequency Variation	Good	Good	Good
Balanced voltage with Sag	Good	Good	Good
Balanced harmonics voltage with sag	Average	Good	Good
Balanced voltage with Swell	Good	Good	Good
Balanced harmonics voltage with swell	Average	Good	Good
Unbalanced voltage with Sag	Good	Good	Good
Unbalanced harmonics voltage with sag	Average	Good	Good
Unbalanced voltage with Swell	Good	Good	Good
Unbalanced harmonics voltage with swell	Average	Good	Good

Among the systems evaluated, DSOGI (Dual Second Order Generalized Integrator) is notable for displaying frequency ripple under these conditions. This frequency ripple leads to tracking errors in the phase angle, compromising the system's ability to accurately synchronize with the reference signal. This indicates that DSOGI struggles to maintain precise phase angle tracking in the presence of substantial harmonic distortion.

In contrast, CDSC (Cascaded Delayed Signal Cancellation) and MDSC (Multiple Delayed Signal Cancellation) demonstrate superior performance. These systems do not exhibit frequency ripple, allowing them to maintain accurate phase angle tracking despite the presence of harmonics. This robustness underscores their effectiveness in managing complex waveforms, ensuring stable and reliable performance even under challenging conditions.

To ensure stable and efficient power system operations, it is crucial to use improved Phase-Locked Loops (PLLs) that perform well under various grid conditions. Table 1 provides a comparative assessment of three advanced PLL techniques: DSOGI, CDSC, and MDSC. Each technique is evaluated based on its efficacy under different grid scenarios, including frequency fluctuation, voltage sag, voltage swell, and the presence of harmonics in both balanced and unbalanced voltage settings.

The performance assessment reveals that while the basic PLL and DSOGI may be effective under certain conditions, they exhibit limitations when dealing with significant harmonic content. Conversely, CDSC and MDSC are more adept at managing a wide range of grid situations, providing robust performance and maintaining high power quality. This comparative analysis highlights the importance of selecting the appropriate PLL approach based on the specific requirements of the power network, particularly in scenarios involving significant harmonic distortion and voltage imbalances. By choosing the right PLL algorithm, it is possible to enhance the stability and efficiency of power system operations, ensuring reliable performance across diverse grid conditions.

DSOGI, CDSC, and MDSC are the three PLL methods that display excellent performance under frequency variation settings. They are able to successfully handle variations in grid frequency while also preserving synchronization and stability. When the grid encounters a voltage sag, all of the approaches perform well, which indicates that they are able to maintain precise phase tracking even when the voltage drops. However, in situations when the grid voltage is sagged and includes harmonics, the performance of the typical PLL declines to an average level. This is because harmonics generate distortions that degrade the precision of phase tracking. On the other hand, DSOGI, CDSC, and MDSC continue to exhibit strong performance, which demonstrates their resilience and their capacity to successfully filter out harmonics.

Table 2. Evaluation of Various parameters of Different PLLs.

Method	Settling Time	Frequency Overshoot	Steady-State Accuracy
FAMAF-PLL	0.035 s	0.4 Hz	Good
MAF-PLL	0.04 s	0.4 Hz	Good
DSOGI-PLL	-	1.3 Hz	Average
CDSC	0.035 s	0.2 Hz	Good
MDSC	0.035 s	0.2 Hz	Good

Three characteristics of the performance of the five PLLs were evaluated and compared: the time required for settling, an overshoot of frequency range, as well as the steady-state precision of the output phase. The table compares five phase-locked loop (PLL) synchronization techniques based on their settling time, frequency overshoot, and steady-state accuracy. FAMAF-PLL has a settling time of 0.035 seconds, indicating quick stabilization after disturbances. Its frequency overshoot is moderate at 0.4 Hz, with good steady-state accuracy, ensuring stable and precise performance. MAF-PLL takes slightly longer to stabilize with a settling time of 0.04 seconds, but it shares the same frequency overshoot of 0.4 Hz and maintains good steady-state accuracy. On the other hand, DSOGI-PLL lacks a specified settling time and exhibits a higher frequency overshoot of 1.3 Hz, suggesting more fluctuation before stabilization and an average level of accuracy. CDSC stands out with a fast settling time of 0.035 seconds and minimal frequency overshoot of 0.2 Hz, indicating high stability and accuracy. Similarly, MDSC matches CDSC's performance, offering the same rapid settling time and low frequency overshoot, with good steady-state accuracy. Overall, CDSC and MDSC provide the best performance, while DSOGI-PLL shows some instability with a higher overshoot and lower accuracy.

During voltage swell circumstances, which are characterized by a transient rise in the magnitude of the voltage, all four approaches once again display excellent performance, managing increases in voltage without losing synchronization. However, because to the standard PLL's susceptibility to harmonic distortions, its performance is assessed as average when the grid voltage includes harmonics and suffers a swell. This is where the conventional PLL's performance stands. The continued success of DSOGI, CDSC, and MDSC is a testament to the sophisticated filtering characteristics of all three systems, which enable them to properly regulate harmonics even while voltage is increasing.

When the three-phase voltages are not equal in magnitude or phase angle, these situations are known as unbalanced voltage conditions. In these settings, all approaches function effectively throughout both sags and swells, ensuring that exact synchronization is maintained. However, when the grid voltage is both unbalanced and includes harmonics during a sag, the performance of the typical PLL is once again mediocre. This is a reflection of the difficulties it encounters with both imbalance and harmonic distortions. In order to demonstrate their complex harmonic mitigation and imbalance management skills, DSOGI, CDSC, and MDSC approaches continue to retain excellent performance.

The performance of the conventional PLL stays average under unbalanced voltage settings with swell and the presence of harmonics. This is because the standard PLL is difficult to manage since it must manage both imbalance and harmonic distortions respectively. Despite their continued success, DSOGI, CDSC, and MDSC continue to demonstrate their sophisticated architecture, which allows them to efficiently handle situations that are so complicated. In conclusion, the typical PLL approach, although its usually good performance under basic grid settings, has a difficult time dealing with harmonic distortions, especially when sags and swells are taken into consideration. The DSOGI, CDSC, and MDSC methods, on the other hand, prove to be the most effective and resilient in guaranteeing stable and dependable grid synchronization in any number of tested scenarios, including those with harmonic distortions and imbalanced voltages.

4. CONCLUSION

The purpose of this paper is to provide a comprehensive analysis of modern Phase-Locked Loops (PLLs) that are designed for accurately extracting Fundamental Frequency Positive Sequence (FFPS) components. The paper focuses specifically on PLLs that are based on Dual Second Order Generalized Integrator (DSOGI), Cascaded Delayed Signal Cancellation (CDSC), and Multiple Delayed Signal Cancellation (MDSC). MATLAB simulations are used to analyze the performance of these sophisticated PLLs under different grid situations in order to determine the effectiveness and resilience of these PLLs. Despite the fact that they do not totally eradicate harmonics, DSOGI-based PLLs are renowned for their capacity to reduce the intensity of harmonics. Due to the presence of harmonics and DC components in the grid voltages, this partial harmonic attenuation results in phase angle tracking performance that is not suitable. since of these limitations, DSOGI is less dependable in contexts where harmonic distortions are severe since it is unable to maintain accurate synchronization under these circumstances.

On the other hand, phase-locked loops (PLLs) that are based on CDSC and MDSC make use of delay operators to completely eliminate some harmonics, which further enhances their capacity to handle grid voltage distortions. In spite of the fact that CDSC and MDSC approaches are not without flaws and let some harmonics to get through without being attenuated, they nonetheless exhibit much superior performance in comparison to DSOGI-based plug-in logic controllers. In the majority of grid circumstances, when CDSC and MDSC-based PLLs are able to maintain correct phase tracking and synchronization, this enhanced performance is especially noticeable. On the other hand, their efficiency decreases when the grid includes dominant harmonics that these PLLs are unable to eliminate. The overall performance of CDSC and MDSC-based PLLs under a variety of grid circumstances is remarkable, leading to the conclusion that these PLLs are typically better than those based on DSOGI. This is despite the fact that this constraint exists. This advantage may be due to their increased skills in eliminating harmonics, which provide grid synchronization that is more dependable and steady.

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APPENDIX

Matlab Function

For phase a

```
function va  = fcn(t,dist,f)
%#codegen
% phase angle difference between a and b
%f = 50;
w1 = 2*pi*f;  % For variable frequency operation
 w = w1;     % Use it for variable freq operation
%w = 2*pi*50; % For constant frequency operation
Vm = 230*sqrt(2); % Peak of source voltage %
if dist == 1        % Normal operation
   va1 = Vm*sin(w*t);
   va5 = 0;
   va7 = 0;
   va11 = 0;
   va13 = 0;
elseif dist == 2      % Balanced voltage sag of 0.5 pu
   va1 = 0.5*Vm*sin(w*t);
   va5 = 0;
   va7 = 0;
   va11 = 0;
   va13 = 0;
elseif dist == 3     % Balanced voltage sag of 0.5 pu with harmonics
   va1 = 0.5*Vm*sin(w*t);
   va5 = 0.2*0.5*Vm*sin(5*w*t)/4;
   va7 = (0.5*Vm*sin(7*w*t))/(7*4);
   va11 = (0.5*Vm*sin(11*w*t))/(11*1);
   va13 = (0.5*Vm*sin(13*w*t))/(13*1);
elseif dist == 4        % Balanced voltage swell of 1.2 pu
   va1 = 1.2*Vm*sin(w*t);
   va5 = 0;
   va7 = 0;
   va11 = 0;
   va13 = 0;
elseif dist == 5     % Balanced voltage swell of 1.2 pu with harmonics
   va1 = 1.2*Vm*sin(w*t);
   va5 = 0.2*1.2*Vm*sin(5*w*t)/4;
   va7 = (1.2*Vm*sin(7*w*t))/(7*4);
   va11 = (1.2*Vm*sin(11*w*t))/(11*1);
   va13 = (1.2*Vm*sin(13*w*t))/(13*1);
elseif dist == 6      % Unbalanced voltage sag of 0.5 pu
   va1 = 0.5*Vm*sin(w*t);
   va5 = 0;
   va7 = 0;
   va11 = 0;
   va13 = 0;
elseif dist == 7     % Unbalanced voltage sag of 0.5 pu with harmonics
   va1 = 0.5*Vm*sin(w*t);
   va5 = 0.2*0.5*Vm*sin(5*w*t)/4;
```

```
    va7 = (0.5*Vm*sin(7*w*t))/(7*4);
    va11 = (0.5*Vm*sin(11*w*t))/(11*1);
    va13 = (0.5*Vm*sin(13*w*t))/(13*1);
elseif dist == 8        % Unbalanced voltage swell of 1.2 pu
    va1 = 1.2*Vm*sin(w*t);
    va5 = 0;
    va7 = 0;
    va11 = 0;
    va13 = 0;
elseif dist == 9      % Unbalanced voltage swell of 1.2 pu with harmonics
    va1 = 1.2*Vm*sin(w*t);
    va5 = 0.2*1.2*Vm*sin(5*w*t)/4;
    va7 = (1.2*Vm*sin(7*w*t))/(7*4);
    va11 = (1.2*Vm*sin(11*w*t))/(11*1);
    va13 = (1.2*Vm*sin(13*w*t))/(13*1);
else
    va1 = Vm*sin(w*t);
    va5 = 0;
    va7 = 0;
    va11 = 0;
    va13 = 0;
end
%}
va = va1 + va5 + va7 + va11 + va13;
```

For phase b

```
function vb  = fcn(t,dist,f)
%#codegen
% phase angle difference between a and b
%f = 50;
w1 = 2*pi*f;  % For variable frequency operation
 w = w1;     % Use it for variable freq operation
%w = 2*pi*50; % For constant frequency operation
Vm = 230*sqrt(2); % Peak of source voltage  %
if dist == 1        % Normal operation
    vb1 = Vm*sin(w*t);
    vb5 = 0;
    vb7 = 0;
    vb11 = 0;
    vb13 = 0;
elseif dist == 2      % Balanced voltage sag of 0.5 pu
    vb1 = 0.5*Vm*sin(w*t);
    vb5 = 0;
    vb7 = 0;
    vb11 = 0;
    vb13 = 0;
elseif dist == 3      % Balanced voltage sag of 0.5 pu with harmonics
    vb1 = 0.5*Vm*sin(w*t);
    vb5 = 0.2*0.5*Vm*sin(5*w*t)/4;
    vb7 = (0.5*Vm*sin(7*w*t))/(7*4);
    vb11 = (0.5*Vm*sin(11*w*t))/(11*1);
    vb13 = (0.5*Vm*sin(13*w*t))/(13*1);
elseif dist == 4        % Balanced voltage swell of 1.2 pu
    vb1 = 1.2*Vm*sin(w*t);
    vb5 = 0;
    vb7 = 0;
    vb11 = 0;
    vb13 = 0;
elseif dist == 5      % Balanced voltage swell of 1.2 pu with harmonics
```

```
    vb1 = 1.2*Vm*sin(w*t);
    vb5 = 0.2*1.2*Vm*sin(5*w*t)/4;
    vb7 = (1.2*Vm*sin(7*w*t))/(7*4);
    vb11 = (1.2*Vm*sin(11*w*t))/(11*1);
    vb13 = (1.2*Vm*sin(13*w*t))/(13*1);
elseif dist == 6      % Unbalanced voltage sag of 0.6 pu
    vb1 = 0.6*Vm*sin(w*t);
    vb5 = 0;
    vb7 = 0;
    vb11 = 0;
    vb13 = 0;
elseif dist == 7      % Unbalanced voltage sag of 0.6 pu with harmonics
    vb1 = 0.6*Vm*sin(w*t);
    vb5 = 0.2*0.6*Vm*sin(5*w*t)/4;
    vb7 = (0.6*Vm*sin(7*w*t))/(7*4);
    vb11 = (0.6*Vm*sin(11*w*t))/(11*1);
    vb13 = (0.6*Vm*sin(13*w*t))/(13*1);
elseif dist == 8        % Unbalanced voltage swell of 1.3 pu
    vb1 = 1.3*Vm*sin(w*t);
    vb5 = 0;
    vb7 = 0;
    vb11 = 0;
    vb13 = 0;
elseif dist == 9      % Unbalanced voltage swell of 1.3 pu with harmonics
    vb1 = 1.3*Vm*sin(w*t);
    vb5 = 0.2*1.3*Vm*sin(5*w*t)/4;
    vb7 = (1.3*Vm*sin(7*w*t))/(7*4);
    vb11 = (1.3*Vm*sin(11*w*t))/(11*1);
    vb13 = (1.3*Vm*sin(13*w*t))/(13*1);
else
    vb1 = Vm*sin(w*t);
    vb5 = 0;
    vb7 = 0;
    vb11 = 0;
    vb13 = 0;
end
%}
vb = vb1 + vb5 + vb7 + vb11 + vb13;
```

For phase c

```
function vc  = fcn(t,dist,f)
%#codegen
% phase angle difference between a and b
%f = 50;
w1 = 2*pi*f;  % For variable frequency operation
 w = w1;     % Use it for variable freq operation
%w = 2*pi*50; % For constant frequency operation
Vm = 230*sqrt(2); % Peak of source voltage  %
if dist == 1        % Normal operation
    vc1 = Vm*sin(w*t);
    vc5 = 0;
    vc7 = 0;
    vc11 = 0;
    vc13 = 0;
elseif dist == 2      % Balanced voltage sag of 0.5 pu
    vc1 = 0.5*Vm*sin(w*t);
    vc5 = 0;
    vc7 = 0;
    vc11 = 0;
```

```
    vc13 = 0;
elseif dist == 3     % Balanced voltage sag of 0.5 pu with harmonics
    vc1 = 0.5*Vm*sin(w*t);
    vc5 = 0.2*0.5*Vm*sin(5*w*t)/4;
    vc7 = (0.5*Vm*sin(7*w*t))/(7*4);
    vc11 = (0.5*Vm*sin(11*w*t))/(11*1);
    vc13 = (0.5*Vm*sin(13*w*t))/(13*1);
elseif dist == 4        % Balanced voltage swell of 1.2 pu
    vc1 = 1.2*Vm*sin(w*t);
    vc5 = 0;
    vc7 = 0;
    vc11 = 0;
    vc13 = 0;
elseif dist == 5     % Balanced voltage swell of 1.2 pu with harmonics
    vc1 = 1.2*Vm*sin(w*t);
    vc5 = 0.2*1.2*Vm*sin(5*w*t)/4;
    vc7 = (1.2*Vm*sin(7*w*t))/(7*4);
    vc11 = (1.2*Vm*sin(11*w*t))/(11*1);
    vc13 = (1.2*Vm*sin(13*w*t))/(13*1);
elseif dist == 6     % Unbalanced voltage sag of 0.7 pu
    vc1 = 0.7*Vm*sin(w*t);
    vc5 = 0;
    vc7 = 0;
    vc11 = 0;
    vc13 = 0;
elseif dist == 7     % Unbalanced voltage sag of 0.7 pu with harmonics
    vc1 = 0.7*Vm*sin(w*t);
    vc5 = 0.2*0.7*Vm*sin(5*w*t)/4;
    vc7 = (0.7*Vm*sin(7*w*t))/(7*4);
    vc11 = (0.7*Vm*sin(11*w*t))/(11*1);
    vc13 = (0.7*Vm*sin(13*w*t))/(13*1);
elseif dist == 8        % Unbalanced voltage swell of 1.4 pu
    vc1 = 1.4*Vm*sin(w*t);
    vc5 = 0;
    vc7 = 0;
    vc11 = 0;
    vc13 = 0;
elseif dist == 9     % Unbalanced voltage swell of 1.4 pu with harmonics
    vc1 = 1.4*Vm*sin(w*t);
    vc5 = 0.2*1.4*Vm*sin(5*w*t)/4;
    vc7 = (1.4*Vm*sin(7*w*t))/(7*4);
    vc11 = (1.4*Vm*sin(11*w*t))/(11*1);
    vc13 = (1.4*Vm*sin(13*w*t))/(13*1);
else
    vc1 = Vm*sin(w*t);
    vc5 = 0;
    vc7 = 0;
    vc11 = 0;
    vc13 = 0;
end
%}
vc = vc1 + vc5 + vc7 + vc11 + vc13;
```

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