Indonesian Journal of Electrical Engineering and Informatics (IJEEI)
Vol. 8, No. 4, December 2020, pp. 666~673
ISSN: 2089-3272, DOI: 10.11591/ijeei.v8i4.2582

High-Performance Design of a 4-Bit Carry Look-Ahead Adder in Static CMOS Logic

Mehedi Hasan [1,2], Abdul Hasib Siddique[1], Abdal Haque Mondol[3], Mainul Hossain[4], Hasan U. Zaman[2], Sharnali Islam[4]

[1]Jack-Kilby VLSI Lab, University of Science and Technology Chittagong, Chattogram 4202, Bangladesh
[2]Department of Electrical and Computer Engineering, North South University, Dhaka 1229, Bangladesh
[3]Department of Electrical and Electronic Engineering, United International University, Dhaka 1212, Bangladesh
Department of Electrical and Electronic Engineering, University of Dhaka, Dhaka 1000, Bangladesh

Article Info

Article history:

Received Jul 1, 2020
Revised Nov 25, 2020
Accepted Dec 10, 2020

Keywords:

4-bit adder
Carry look-ahead adder
Parallel-prefix adder
Carry-generate
Carry-propagate

ABSTRACT

Design of a 4-bit Carry Look-Ahead (CLA) process in static CMOS logic has been presented. CLA architecture proposed in this work computes carry-out terms without using carry-propagate and carry-generate signals which are used in conventional static CMOS (C-CMOS) 4-bit CLA adder. Performance parameters of the proposed 4-bit CLA architecture have been simulated and validated by comparing with the conventional design using Cadence design toolset in 45 nm technology. The designs were compared in terms of average power consumption, propagation delay and power delay product (PDP). The proposed 4-bit CLA topology obtained 34.53 % improvement in speed, 4.84 % improvement in power consumption and 37.696 % improvement in PDP while the source voltage was 1.0 V. Hence, as per acquired simulation results, the proposed 4-bit CLA structure is proven to be an excellent alternative to the conventional design for data-path design in modern high-performance processors.

Corresponding Author:

Mehedi Hasan
Jack-Kilby VLSI Lab,
University of Science and Technology Chittagong
Zakir Hossain Road, Foy's Lake, Khulshi, Chattogram 4202, Bangladesh.
Email: mehedi.hasan01@northsouth.edu

1. INTRODUCTION

The necessity of high-speed, energy-saving and area-efficient way of arithmetic operations has become the foremost requirements for present-day microprocessors. Among the arithmetic operations, addition of binary numbers plays the most prominent role since many other arithmetic operations require addition to compute [1]. Moreover, addition plays a critical role in crypto-processing, parallel-processing and digital signal processing for which adder design with excellent performance parameters has gained paramount interest among researchers [2].

In the traditional way of implementing wide adder in Ripple Carry Adder (RCA) style, computation in one stage needs to wait for the carry-out bit from the previous stage [3]. Among high-speed wide adder topologies, the CLA process prevails dominant as the delay occurred due to carry propagation is reduced by computing several stages in parallel [4]. Architecture of 4-bit CLA process plays an important role in wide adder design since 4-bit adders are used as fundamental units [5]. Hence, optimized high-performance design of a 4-bit CLA process will bring about comprehensive performance enhancement in wide adder blocks [6].

Although various CLA techniques mainly focused in CLA logic interpretation and algorithms have been developed, only a handful amount of research work has been conducted in transistor level representation of 4-bit CLA. In this work, a transistor level static CMOS logic based CLA process for generating carry-out

bits of 4-bit CLA adder has been proposed. The proposed CLA circuit design computes carry-out bits without using the traditional method of generating carry-generate and carry-propagate terms. Rather, complex transistor networks have been developed in order to reduce delay and power.

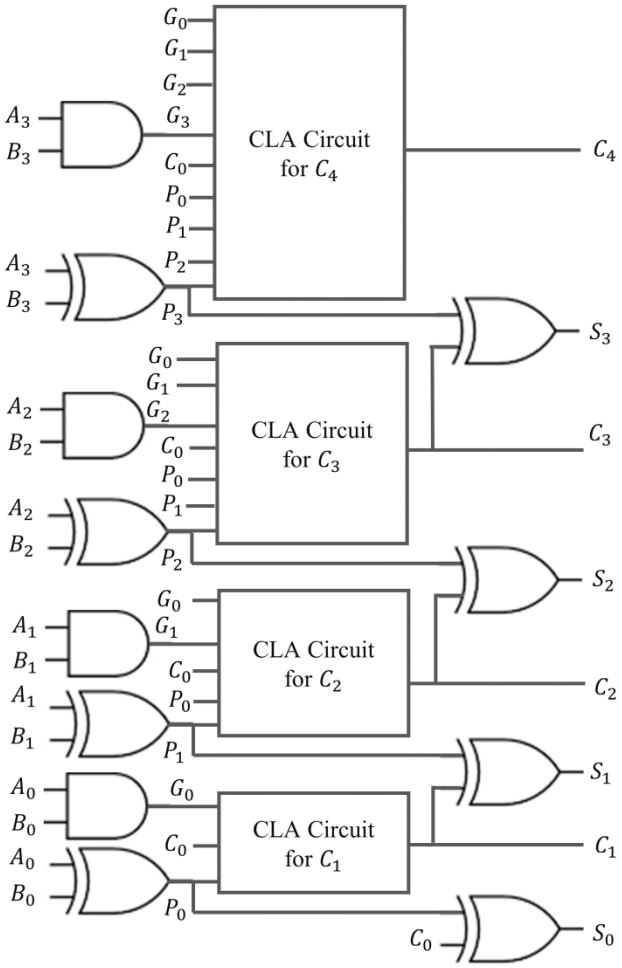

Figure 1. Logic gate level representation of conventional static CMOS 4-bit CLA adder.

2. CONVENTIONAL 4-BIT CLA PROCESS IN STATIC CMOS LOGIC

Conventional execution of CLA adder uses carry-generate (G_i) and carry-propagate terms (P_i) [7-8]. If the input bits are denoted as A_i and B_i, then G_i and P_i terms can be expressed as the following equations.

$$G_i = A_i B_i \quad (1)$$

$$P_i = A_i \oplus B_i \quad (2)$$

Now, as per reference [9], carry-out bits for CLA adder can be written in general as:

$$C_{i+1} = G_i + P_i C_i \quad (3)$$

Using equation (1), (2) and (3), carry-out equations for 4-bit CLA can be written as [9]:

$$C_1 = G_0 + P_0 C_0 \quad (4)$$

$$C_2 = G_1 + P_1 C_1$$
$$= G_1 + P_1 G_0 + P_1 P_0 C_0 \quad (5)$$

$$C_3 = G_2 + P_2 C_2$$
$$= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \quad (6)$$

$$C_4 = G_3 + P_3 C_3$$
$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0 \quad (7)$$

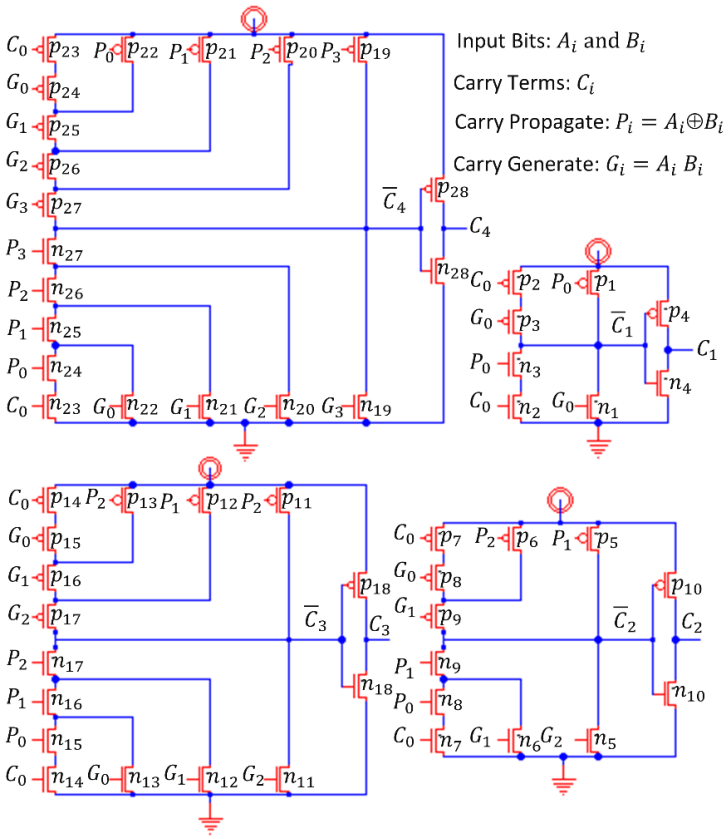

Figure 2. Transistor level representation of conventional static CMOS 4-bit CLA adder.

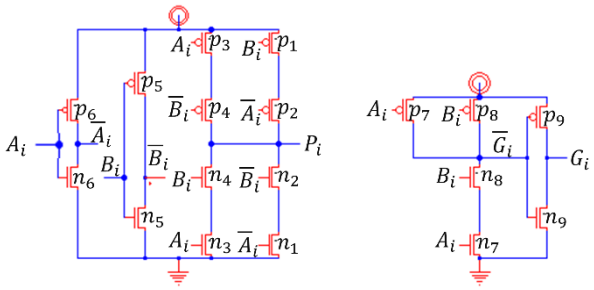

Figure 3. Transistor level representation of XOR and AND gate used in conventional static CMOS CLA process for generating G_i and P_i signals.

As per the above equations and information about conventional CLA process provided in reference [10], logic gate level representation of 4-bit CLA adder can be expressed using Fig. 1. Now, using equations (4), (5), (6) and (7), switch level (transistor level) CLA circuits (for C_1, C_2, C_3 and C_4) in Fig. 1 have been expressed in reference [4, 11-13]. Conventional CLA circuits for computing carry-out terms have been represented by Fig. 2. For the input signals (P_i and G_i) of CLA circuits in Fig. 2, conventional design uses AND and XOR gate depicted in Fig. 3.

3. PROPOSED 4-BIT CARRY LOOK-AHEAD ADDER IN STATIC CMOS LOGIC

The proposed CLA technique, as shown in Fig. 4 computes carry-out bits without P_i and G_i terms. In the proposed design, all input bits are directly used as inputs in the CLA circuits for carry generation. Sum Generation part is exactly the same as the conventional design. In order to design the CLA circuits in terms of the input bits (A_i, B_i and C_0), it is necessary to derive the simplified Boolean equations in terms of the input bits. The simplified Boolean equations for the proposed design are:

$$C_1 = C_0(A_0 + B_0) + A_0B_0 \quad (8)$$

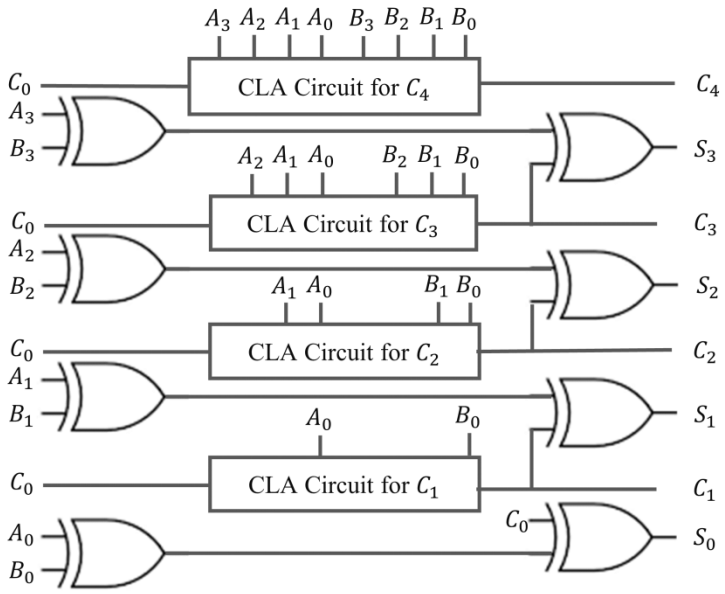

Figure 4. Logic gate level representation of proposed static CMOS CLA adder.

$$C_2 = (C_0(A_0 + B_0) + A_0B_0)(A_1 + B_1) + A_1B_1$$
$$= C_1(A_1 + B_1) + A_1B_1 \quad (9)$$
$$C_3 = (C_1(A_1 + B_1) + A_1B_1)(A_2 + B_2) + A_2B_2$$
$$= C_2(A_2 + B_2) + A_2B_2 \quad (10)$$
$$C_4 = (C_2(A_2 + B_2) + A_2B_2)(A_3 + B_3) + A_3B_3$$
$$= C_3(A_3 + B_3) + A_3B_3 \quad (11)$$

Hence, in general, carry-out bits can be written as:

$$C_{i+1} = C_i(A_i + B_i) + A_iB_i \quad (12)$$

Although the equations (8)-(12) is similar to equations of 4-bit Ripple Carry Adder (RCA), the transistor level design methodology presented in this section will transform the RCA equations into CLA process. With thorough scrutiny of equations (8)-(12), it can be observed that the preceding carry-out bit circuit for C_i works as a fundamental building unit for its next carry-out bit C_{i+1}. Therefore, the first step is to implement C_1. Implementation of N-channel CMOS (NMOS) network requires series connection of NMOS for AND operation (A_0B_0) and parallel connection of NMOS for OR operation (A_0+B_0) [14]. Now, it can be observed from equation (8) that A_0+B_0 is having AND operation with C_0. Therefore, C_0 has been added in series with A_0+B_0 network to implement $C_0(A_0+B_0)$. Further analysis of equation (8) would reveal that $C_0(A_0+B_0)$ is having OR operation with A_0B_0. Hence, network for A_0B_0 and $C_0(A_0+B_0)$ are implemented in parallel (denoted by circuit 1 in Fig. 5). Now, in order to construct the sub-sequent NMOS network circuit for C_2, circuit 1 would be used as a base. It can be easily understood for equation (9) that A_1+B_1 would be in series with NMOS network of circuit `1 which implements $C_1(A_1+B_1)$. Later, A_0B_0 network has been added in parallel with $C_1(A_1+B_1)$ to construct NMOS network (denoted by circuit 2 in Fig. 5) required for C_2. Using exactly the same procedure, NMOS networks required for C_3 (denoted by circuit 3 in Fig. 5) and C_4 (denoted by circuit 4 in Fig. 5) have been constructed by using equations (10) and (11) respectively. Next, to provide full swing output, pull-up network using P-channel CMOS (PMOS) network is needed to be constructed. Since the number of input combinations that produce '0' and the number of input combinations that produce '1' are equal in carry-generation block of adder circuits, PMOS network for pull-up would be the mirror replica of NMOS networks [7, 15]. In this technique, since PMOS and NMOS networks mirror replica of each other, the overall circuit becomes symmetric. Complete schematic of carry-generation circuits has been represented by Fig. 6. Since static CMOS logic provides complementary output, it is necessary to invert the logic level to get the desired output [7]. Therefore, inverters have been added to the design in order to get carry-out signals.

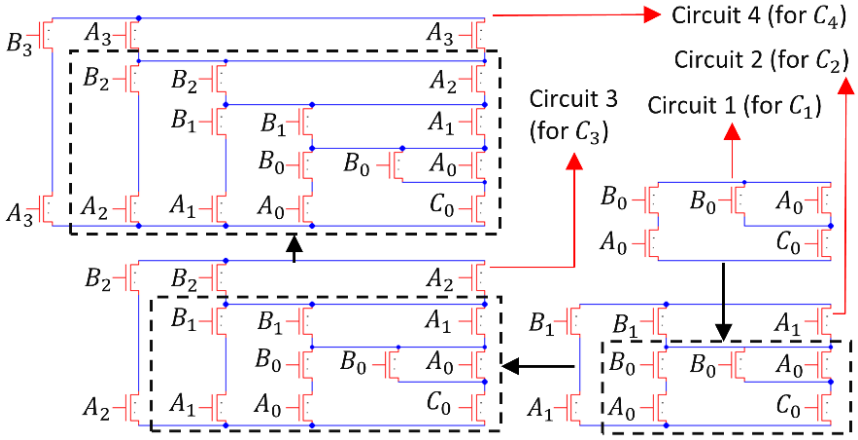

Figure 5. NMOS network implementation process for proposed 4-bit CLA.

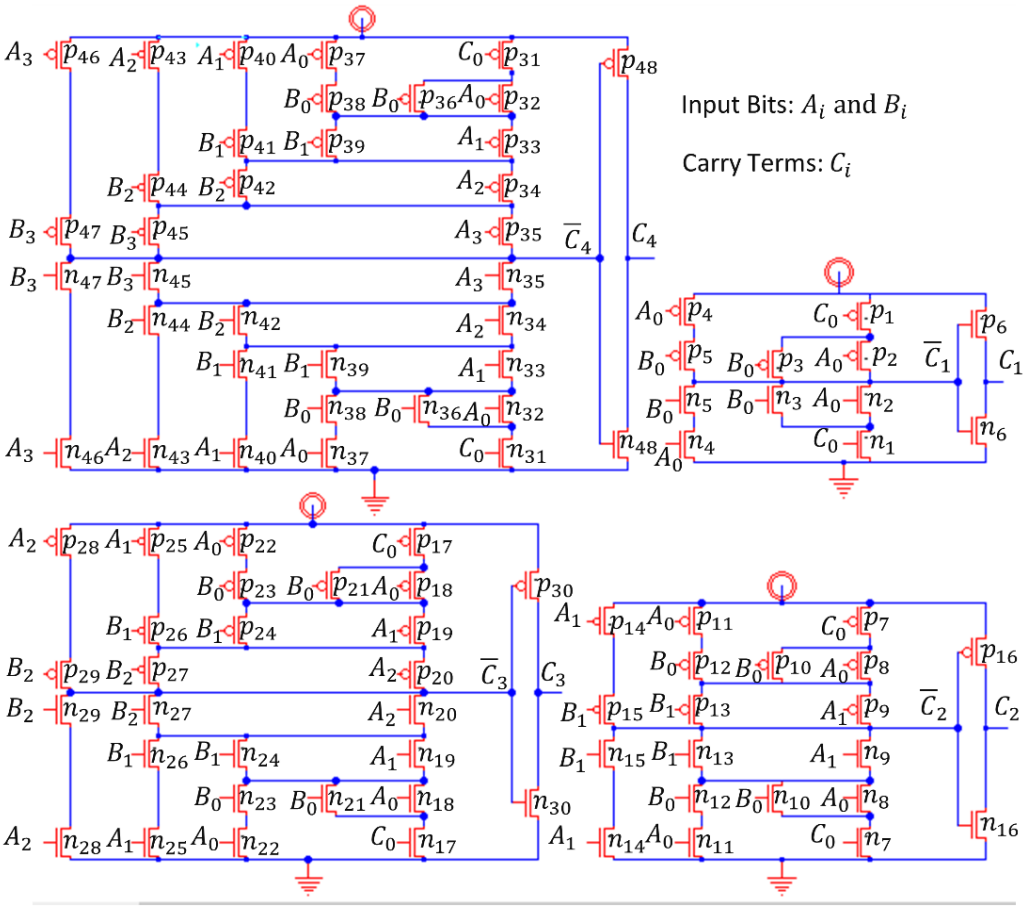

Figure 6. Transistor level representation of proposed static CMOS CLA circuits for carry-out bits.

For sum generation, input signals A_i and B_i are used as inputs to XOR gate depicted in Fig. 3. This provides the P_i signals. Later, P_i and C_i signals are used as input to another set of XOR gates to compute sum signals (S_i). This sum generation process in Fig. 4 is the exact equivalent to the process in conventional design in Fig. 1. Hence, the proposed design has only made changes in the design methodology of the CLA circuits whereas the sum generation process has been kept exactly the same as the conventional one.

4. SIMULATION RESULT ANALYSIS AND COMPARISON

To determine the improvement the proposed 4-bit CLA Adder can bring, the proposed and the conventional design topologies are required to be implemented, simulated and compared. In order to do so, simulation has been conducted utilizing Cadence design and simulation tools with the technology node of 45 nm. The source voltage used is 1 V. Transistor sizes used to implement the VLSI circuits in Fig. 2, Fig. 3 and Fig. 6 are mentioned in Table 1. Post-layout simulation results for the adders are discussed in the following paragraphs.

Key performance parameters: average power, propagation delay and power delay product have been evaluated and compared. To calculate average power, every single combination of the input signals has been applied to the 4-bit adder designs and power consumption has been computed for each case. Then, the average value of the obtained power consumption for all simulation data has been determined as average power. As per Table 2, the proposed design accomplished 4.84 % improvement in power consumption. Dynamic power in integrated circuit is the major contributor to the overall power consumption which occurs due to transitions of logic gates [16-18]. The proposed 4-bit CLA adder reduced dynamic power by completely eliminating the AND gates (G_i terms) from the design. Since the number of logic gates has been reduced, the proposed design experiences less transition occurrence for which dynamic power consumption has been reduced. As a result, overall improvement of power could be accomplished in this research.

In addition to the improvement in average power, the proposed 4-bit CLA adder made 34.53 % improvement in propagation delay. In a VLSI circuit, there can be two types of critical path: rise time critical path and fall time critical path. Critical path rise time means the transistor path due to which maximum rise time delay occurs. On the other hand, Critical path fall time means the transistor path due to which maximum fall time delay occurs. Critical path rise time and fall time delay graphs (proposed and conventional) have been depicted in Fig. 7. Propagation delay for rise and fall time have been determined by calculating the time from 50% of input signal to 50% of output signal swing. Later, the average of propagation delays for rise and fall time graphs has been taken as the final propagation delay. Now, if we analyze Fig. 1 and Fig. 4 carefully, it can be clearly visualized that the inputs to the CLA circuits in conventional design come from AND and XOR gates whereas the inputs to the proposed CLA circuits are the input bits (A_i and B_i) themselves. Since the AND and XOR gates have their own delays which are obviously not negligible, the CLA circuits in the conventional design receive the input signals (P_i and G_i) a bit later than the proposed CLA circuits. This enabled the proposed CLA circuits to compute faster than the conventional ones. The improvement in power and delay resulted in 37.696 % improvement in PDP. Thus, the proposed 4-bit CLA Adder can be considered as an excellent substitute of the conventional one due to its enhanced performance in speed and power.

Table 1. Transistor sizes of devices in Fig. 2, Fig. 3 and Fig. 6

Transistor Sizes of NMOS and PMOS in Fig. 2			
Transistor Number	***Channel Width (nm)***	***Transistor Number***	***Channel Width (nm)***
$n_1, n_5, n_6, n_{11}, n_{12}, n_{13}, n_{19}, n_{20}, n_{21}, n_{22}, n_4, n_{10}, n_{14}, n_{28}$	120	$p_1, p_5, p_6, p_{11}, p_{12}, p_{13}, p_{19}, p_{20}, p_{21}, p_{22}, p_4, p_{10} p_{14}, p_{28}$	160
n_2, n_3	160	p_2, p_3	240
n_7, n_8, n_9	240	p_7, p_8, p_9	360
$n_{14}, n_{15}, n_{16}, n_{17}$	320	$p_{14}, p_{15}, p_{16}, p_{17}$	480
$n_{23}, n_{24}, n_{25}, n_{26}, n_{27}$	400	$p_{23}, p_{24}, p_{25}, p_{26}, p_{27}$	600
Transistor Sizes of NMOS and PMOS in Fig. 3			
Transistor Number	Channel Width (nm)	Transistor Number	Channel Width (nm)
n_5, n_6, n_9	120	p_5, p_6, p_7, p_8, p_9	160
$n_1, n_2, n_3, n_4, n_7, n_8$	160	p_1, p_2, p_3, p_4	240
Transistor Sizes of NMOS and PMOS in Fig. 6			
Transistor Number	***Channel Width (nm)***	***Transistor Number***	***Channel Width (nm)***
$n_6, n_{16}, n_{30}, n_{48}$	120	$n_6, n_{16}, n_{30}, n_{48}$	160
$n_1, n_2, n_3, n_4, n_5, n_{14}, n_{15}, n_{25}, n_{26}, n_{28}, n_{29}, n_{40}, n_{41}, n_{43}, n_{44}, n_{46}, n_{47}$	160	$n_1, n_2, n_3, n_4, n_5, n_{14}, n_{15}, n_{25}, n_{26}, n_{28}, n_{29}, n_{40}, n_{41}, n_{43}, n_{44}, n_{46}, n_{47}$	240
$n_7, n_8, n_9, n_{10}, n_{11}, n_{12}, n_{13}$	240	$n_7, n_8, n_9, n_{10}, n_{11}, n_{12}, n_{13}$	360
$n_{17}, n_{18}, n_{19}, n_{20}, n_{21}, n_{22}, n_{23}, n_{24}, n_{27}$	320	$n_{17}, n_{18}, n_{19}, n_{20}, n_{21}, n_{22}, n_{23}, n_{24}, n_{27}$	480
$n_{31}, n_{32}, n_{33}, n_{34}, n_{35}, n_{36}, n_{37}, n_{38}, n_{39}, n_{42}, n_{45}$	400	$n_{31}, n_{32}, n_{33}, n_{34}, n_{35}, n_{36}, n_{37}, n_{38}, n_{39}, n_{42}, n_{45}$	600
All PMOS and NMOS transistors have 45 nm channel length			

Table 2. Performance comparison of 4-bit CLA adders in static CMOS logic

4-Bit CLA Adder Cell	Transistor Count	Average Power (µW)	Propagation Delay (ns)	PDP (fJ)
Conventional	170	7.85	0.0895	0.703
Proposed	186	7.47	0.0586	0.438
Improvement	------	4.84%	34.53%	37.696%

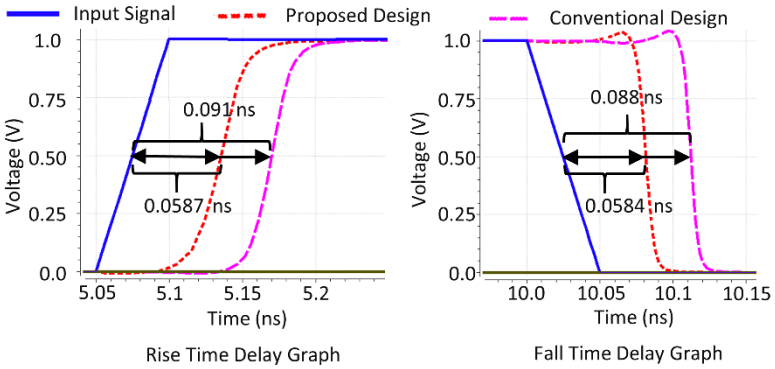

Figure 7. Rise time delay and fall time delay for critical path.

In modern high-speed microprocessors, 4-bit adder architectures are taken as basic building block in order to implement higher order adders (for example 16-bit, 32-bit, 64-bit, etc.) [5]. Therefore, if the 4-bit base circuit have good performance parameters, then the effect of utilizing the 4-bit base in higher order adders will bring oveall performance improvement. Thus, the main goal of this research was to design a 4-bit adder block for using as a building block in higher order adders. Full Adder (FA) based 32-bit Ripple Carry Adder (RCA) in [2] has high delay because of having long carry propagation chain. To overcome this, parallel adder methodologies have evolved among which CLA is quite popular. The carry-generation circuit of 4-bit CLA in [4] is exactly similar to the carry-generation circuit of conventional 4-bit CLA in Fig. 2. Hence, this research only displayed a comparison of the proposed 4-bit CLA with the conventional design. Since the proposed 4-bit design shows better performance, the effect of using it as a base to build higher order adder (16-bit, 32-bit, 64-bit, etc.) will bring about extensive performance enhancement.

4. CONCLUSION

A 4-bit CLA process in static CMOS logic has been developed in this research work. The CLA process generates carry-out terms without utilizing the P_i and G_i terms which are used in conventional design. The feasibility and effectiveness of the proposed design have been evaluated by comparing it with the conventional design of 4-bit CLA adder in static CMOS logic. The improvements were done in average power, propagation delay and PDP are 4.84 %, 34.53 % and 37.696 % respectively which makes the proposed design quite effective in modern high-performance integrated circuit design.

REFERENCES

[1] M. Hasan, M. J. Hossein, U. K. Saha and M. S. Tarif, "Overview and Comparative Performance Analysis of Various Full Adder Cells in 90 nm Technology," 2018 4th International Conference on Computing Communication and Automation (ICCCA), Greater Noida, India, 2018, pp. 1-6.

[2] M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman and S. Islam, "Design of a Scalable Low-Power 1-Bit Hybrid Full Adder for Fast Computation," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 8, pp. 1464-1468, 2020.

[3] V. Pudi and K. Sridharan, "Low Complexity Design of Ripple Carry and Brent–Kung Adders in QCA," IEEE Transactions on Nanotechnology, vol. 11, no. 1, pp. 105-119, 2012.

[4] M. Hasan, M. S. Islam, M. R. Ahmed, "Performance improvement of 4-bit static CMOS carry look-ahead adder using modified circuits for carry generate and propagate terms," Science Journal of Circuit, Systems and Signal Processing, vol. 8, no. 2, pp. 76-81, 2019.

[5] P. Balasubramanian, M. Mastorakis "Performance comparison of carry look-ahead and carry-select adders based on accurate and approximate additions," *Electronics*, vol. 7, no. 12, pp. 369-381, 2018.

[6] R. Johri, S. Akashe, S. Sharma "High-performance 8-bit cascaded carry look-ahead adder with precise power consumption," *International Journal of Communication Systems*, vol. 28, pp. 1475-1483, 2014.

[7] N. H. E. Weste, D. Harris, and A. Banerjee, CMOS VLSI Design: A Circuits and Systems Perspective, 3rd ed. Delhi, India: Pearson Education, 2010.

[8] R. Zlatanovici, S. Kao and B. Nikolic, "Energy–Delay Optimization of 64-Bit Carry-Lookahead Adders With a 240 ps 90 nm CMOS Design Example," IEEE Journal of Solid-State Circuits, vol. 44, no. 2, pp. 569-583, Feb. 2009.

[9] M. Valinataj, "Fault-tolerant carry look-ahead adder architectures robust to multiple simultaneous errors," Microelectronics Reliability, vol. 55, no. 12, pp. 2845-2857, 2015.

[10] A. Ibrahim, F. Gebali, "Optimized structure of hybrid ripple carry and hierarchical carry lookahead adders," Microelectronics Journal, vol. 46, no. 9, pp. 783-794, 2015.

[11] M. Binggeli, S. Denton, N. S. Muppaneni and S. Chiu, "Optimizing carry-lookahead logic through a comparison of PMOS and NMOS block inversions," 2015 IEEE International Conference on Electro/Information Technology (EIT), Dekalb, IL, 2015, pp. 641-646.

[12] S. Perri, M. Lanuzza, P. Corsonello, "Design of high-speed low-power parallel-prefix adder trees in nanometer technologies," International Journal of Circuit Theory and Applications, vol. 42, pp. 731-743, 2014.

[13] S. Ghafari, M. Mousazadeh, A. Khoei, A. Dadashi, "A new high-speed and low area efficient pipelined 128-bit adder based on modified carry look-ahead merging with Han-Carlson tree method," 2019 MIXDES-26th International Conference on Mixed Design in Integrated Circuits and Systems, Rzeszow, Poland, June 2019, pp. 157-162.

[14] A. Pal, "Low-power VLSI circuits and systems," Springer, New Delhi, India, 2015.

[15] B. R. Zeydel, D. Baran and V. G. Oklobdzija, "Energy-Efficient Design Methodologies: High-Performance VLSI Adders," IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1220-1233, June 2010.

[16] M. Hasan, H. U. Zaman, M. Hossain, P. Biswas, S. Islam, "Gate diffusion input technique based full swing and scalable 1-bit hybrid full adder for high performance applications," Engineering Science and Technology, an International Journal, vol. 23, no. 6, pp. 1364-1373, 2020.

[17] S. Chandra, K. Lahiri, A. Raghunathan and S. Dey, "Variation-Tolerant Dynamic Power Management at the System-Level," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 17, no. 9, pp. 1220-1232, Sept. 2009.

[18] M. Hasan, U. K. Saha, A. Sorwar, M. A. Z. Dipto, M. S. Hossain and H. U. Zaman, "A Novel Hybrid Full Adder Based on Gate Diffusion Input Technique, Transmission Gate and Static CMOS Logic," 2019 10th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Kanpur, India, 2019, pp. 1-6.